Fuji Switching Power Control IC

FA5526/5527/5528
FA5536/5537/5538

Application Note

April.-2011
Fuji Electric Co., Ltd.

Warning

1. This Data Book contains the product specifications, characteristics, data, materials and structures as of April in 2011. The contents are subject to change without prior notice for specification changes or other reasons. When using a product listed in this Data Book, be sure to obtain the latest specifications and check the data.

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   - Measurement equipment ・Machine tools ・Audiovisual equipment
   - Electrical home appliances ・Personal equipment ・Industrial robots, etc.

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   - Traffic-signal control equipment ・Gas leakage detectors with an auto-shutoff function
   - Disaster prevention / security equipment ・Safety devices

6. Do not use a product in this Data Book for equipment requiring extremely high reliability such as:
   - Space equipment ・Airborne equipment ・Atomic control equipment
   - Submarine repeater equipment ・Medical equipment

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Contents

Note）

- The contents of this Data Book are subject to change without prior notice for improvement or other reasons.
- Application examples and parts constants listed in this Data Book are intended for design reference, without giving due consideration to unevenness in parts characteristics and usage conditions.
  When using, be sure to design the relevant circuit giving due consideration to unevenness in parts characteristics and usage conditions.

1. Outline

FA5526/27/28/36/37/38 series are current-mode switching power control ICs that can directly drive power MOSFETs. Low-power dissipation is achieved due to adoption of high break-down voltage CMOS process. In addition, stand-by power consumption can substantially be reduced due to a built-in start-up circuit. Many functions are incorporated in an eight pin package, reducing the number of external parts and allowing compact and high cost performance power supply

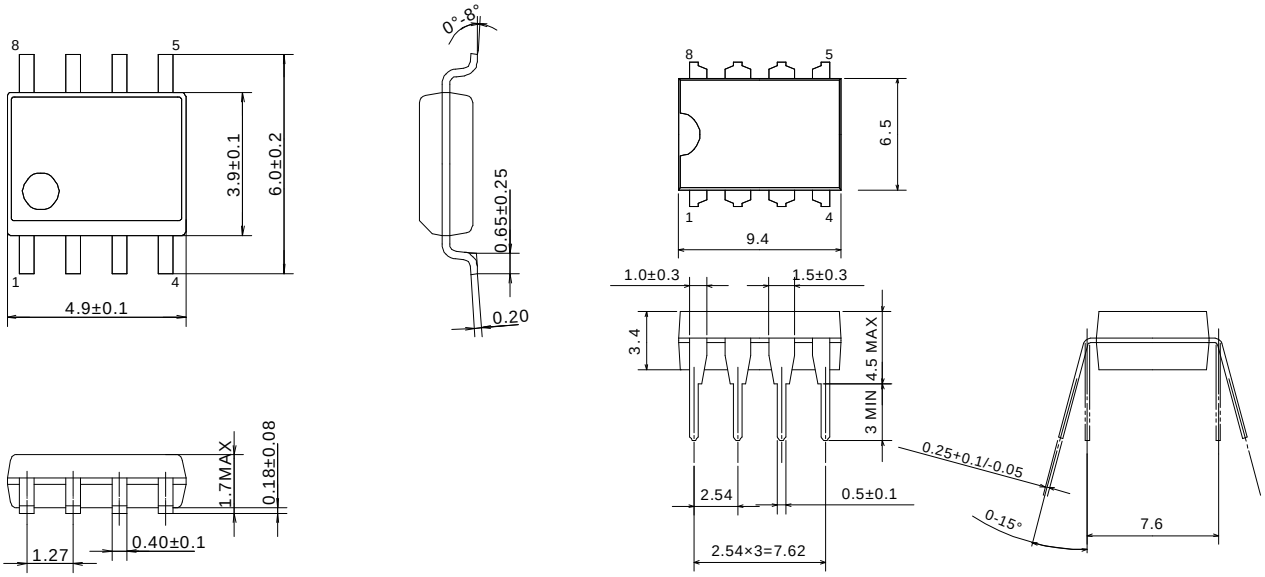
2. Features

- Built-in start-up circuit of 500V break-down voltage that is cut off after start-up (input current after cutoff: 25μA (typ.))
- Low power dissipation due to adoption of high break-down voltage CMOS process
  Supply Current in Operating Mode : 1.4mA (typ.)　(for FA5528 and FA5538)
- Built-in frequency-decreasing function at light load
- Oscillating frequency
  FA5526/5536 : 130kHz(typ.), FA5527/5537 : 100kHz(typ.), FA5528/5538 : 60kHz(typ.)
- Built-in latch-mode cutoff function of overload (over current) for FA5526/5527/5528
- Built-in Auto-Recovery cutoff function of overload (over current) for FA5536/5537/5538
- Built-in latch-mode cutoff function of over-voltage for 28V(typ.) at VCC pin for FA5526/5527/5528.
- Built-in Auto-Recovery-mode cutoff function of over-voltage for 28V(typ.) at VCC pin for FA5536/5537/5538.
- Built-in Under Voltage Lock-Out for VCC pin (15V : ON, 9V : OFF)
- 8 pins package(DIP / SO)

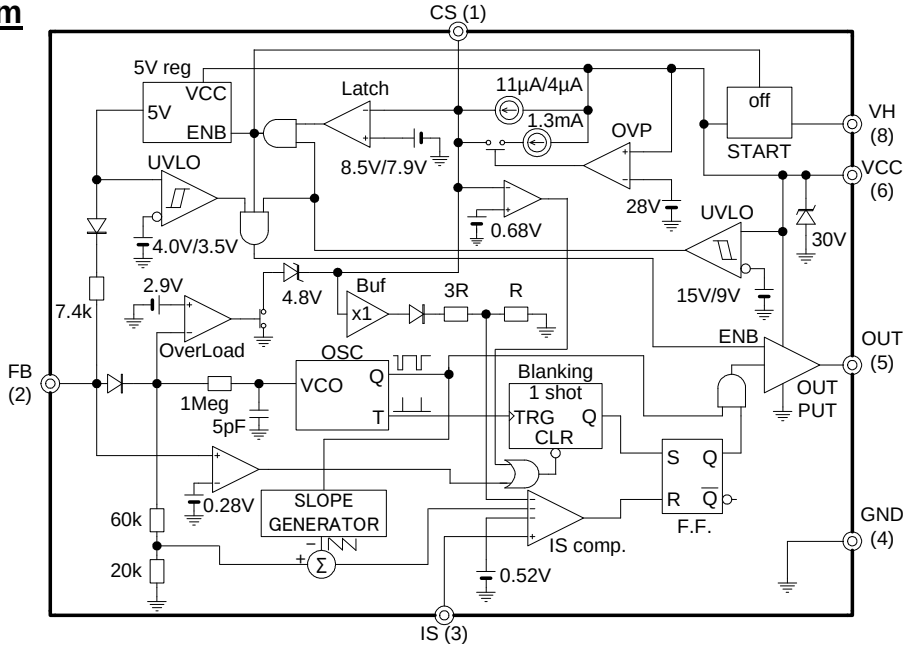
3. External dimension diagram

Unit：mm

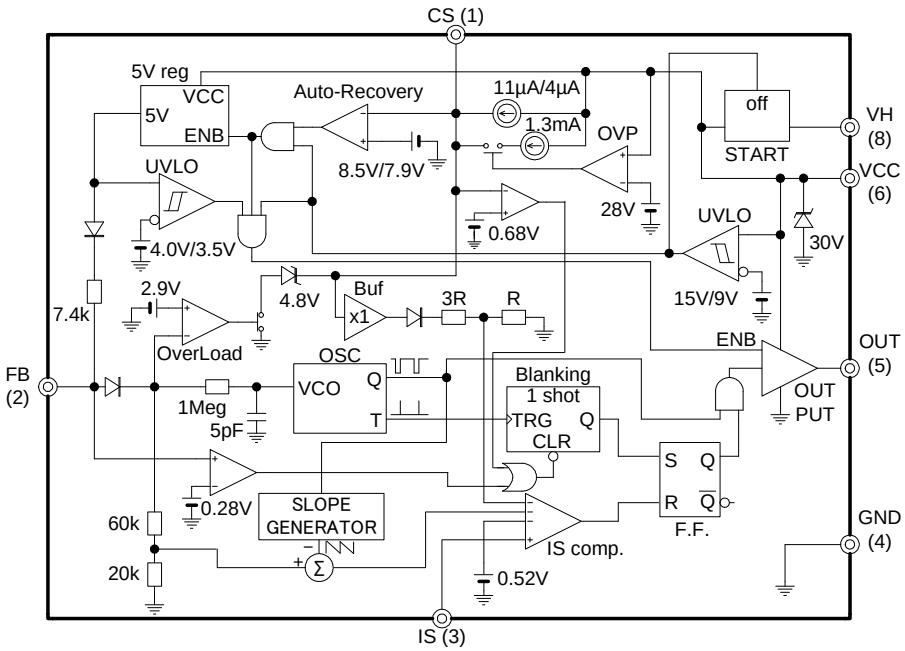
SO-8　（FA5526N/27N/28N/36N/37N/38N）　　DIP-8　（FA5526P/27P/28P/36P/37P/38P）



4. Block diagram



FA5526 / FA5527 / FA5528 for Timer Latched OCP



FA5536 / FA5537 / FA5538 for Auto-Recovery OCP

5. Pin assignments

Pin	Symbol	Function	Description
1	CS	Soft start/latch-mode stop	Time Setting of Soft start and Over Current Protection
2	FB	Feedback input	Input for controlling current comparator threshold voltage
3	IS	Current sensor input	Input for monitoring MOSFET current
4	GND	Ground	Power supply ground
5	OUT	Output	Output for directly driving a MOSFET
6	VCC	Power supply	Power supply for ICs
7	(NC)	No connection	No connection
8	VH	High voltage input	Input terminal for start-up circuit

6. Line-up of FA5526/27/28/36/37/38 series

Type	Switching Frequency (kHz)	Over Current Protection	Package
FA5526P/N	130 (typ.)	Latch with adjustable delay time	DIP-8/SO-8
FA5527P/N	100 (typ.)	Latch with adjustable delay time	DIP-8/SO-8
FA5528P/N	60 (typ.)	Latch with adjustable delay time	DIP-8/SO-8
FA5536P/N	130 (typ.)	Auto-Recovery	DIP-8/SO-8
FA5537P/N	100 (typ.)	Auto-Recovery	DIP-8/SO-8
FA5538P/N	60 (typ.)	Auto-Recovery	DIP-8/SO-8

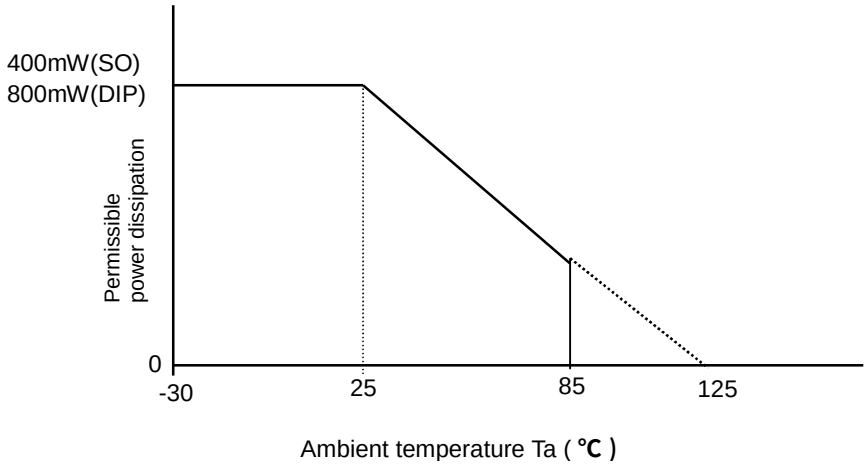
7. Ratings and characteristics

＊In defining a current, “＋” represents a sink current and “－” a source current.

(1) Absolute maximum ratings

Item		Symbol	Rating	Unit
Supply voltage	Low impedance source (Icc>15mA)	V_{CC1}	28	V
	Built-in Zener clamp (Icc<15mA)	V_{CC2}	Self Limiting	V
OUT pin peak current		I_{OH}	-0.3	A
		I_{OL}	+0.6	A
OUT pin voltage		V_{OUT}	-0.3 to VCC+0.3	V
FB/ IS pin voltage		V_{LT}	-0.3 to 5.0	V
CS pin sink current		I_{CS}	2.0	mA
CS pin minimum voltage		V_{CSL}	-0.3	V
VH pin Voltage		V_{VH}	-0.3 to 500	V
Total power dissipation (Ta=25℃)		Pd	800 (DIP-8) 400 (SO-8)	mW
Ambient temperature		Ta	-30 to +85	**degree**
Maximum junction temperature		Tj	125	**degree**
Storage temperature		Tstg	-40 to +150	**degree**

Permissible power dissipation decreasing characteristics



(2) Recommended operating conditions

Item		Symbol	MIN	TYP	MAX	Unit
Supply voltage		V_{CC}	10	18	26	V
VH pin voltage	DC Voltage	$V_{VH(DC)}$	80		450	$V_{(DC)}$
	AC Line Voltage	$V_{VH(AC)}$	80		288	$V_{(AC)}$
VH pin series resistor		R_{VH}	2.2		47	k ohm
CS pin capacitor		C_{CS}	0.01		1	µF
VCC pin capacitor		C_{VCC}	10	33		µF

(3) Electrical characteristics (Vcc=18V, Tj=25℃, unless otherwise specified)

Oscillator (FB pin)

Item	Symbol	Condition		MIN	TYP	MAX	Unit
Oscillating frequency	Fosc	FB=3V	FA5526/36	117	130	143	kHz
			FA5527/37	90	100	110	
			FA5528/38	54	60	66	
Supply voltage stability	Fdv	Vcc = 10 to 26V		-2		2	%
Temperature stability	FdT	Ta = -30 to 85℃			+0.025		%/℃
FB pin voltage for starting frequency variation	VfbM			0.95	1.05	1.15	V
Frequency reduction ratio	kf	⊿I/⊿VFB at FB pin =0.8V to 0.9V	FA5526/36		310		kHz/V
			FA5527/37		240		
			FA5528/38		140		
Oscillating frequency at light load	F06	FB pin =0.6V	FA5526/36		1.1		kHz
			FA5527/37		1.1		
			FA5528/38		1.1		
Minimum frequency *1	Fmin			0.4	1.1	3.0	kHz

*1 The frequency become much smaller than 1.1kHz when intermittent switching occurs at light load near no load.

Pulse width modulator (FB pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Maximum duty cycle	D_{MAX}	FB pin = 3V, CS pin = 3V	76	80	84	%
Minimum duty cycle	D_{MIN}	FB pin = 0V, CS pin = 3V			0	%
FB voltage for pulse stop	V_{THFB0}	Duty cycle = 0%	200	280	360	mV
FB pin current	I_{fb0}	FB pin = 0V	-620	-520	-420	uA

Current sensor (IS pin)

Item	Symbol	Condition		MIN	TYP	MAX	Unit
Voltage gain	AVIS	⊿/FB/⊿/IS		3.8	4.0	4.2	V/V
Maximum threshold voltage	VthIS1	FB pin = 4V, duty = 10%		470	520	570	mV
Slope compensation value	SLP	FB pin=4V	FA5526/36		-24		mV/us
			FA5527/37		-17		
			FA5528/38		-12		
Minimum ON pulse width	Tmin	FB pin=3V CS pin=0V IS pin=1V	FA5526/36		0.3		us
			FA5527/37		0.5		
			FA5528/38		0.7		
Blanking time	Tblank		FA5526/36		0.2		us
			FA5527/37		0.4		
			FA5528/38		0.6		
Output delay time	TpdIS	IS pin to OUT pin			100		ns

Soft-start circuit (CS pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Charging current	ICS0	CS pin = 0V	-15	-11	-5	uA
Threshold voltage for changing charging current	VTHCS1	Ics = -12 ←→ -4μA		3		V
Input threshold voltage	VTHCS0	OUT pin width = Tmin, FB pin = 3V		0.68		V

Over Current Protection circuit (CS pin) : Latch OFF for FA5526/27/28 and Auto-Recovery for FA5536/37/38

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Charging current	ICS4	CS pin = 4V	-6	-4	-2	uA
Sink current	Isink	CS pin = 6V	34	59	84	uA
Cutoff threshold voltage	VTHCSF	ON→OFF	8.0	8.5	9.0	V
	VTHCSN	OFF→ON	7.4	7.9	8.4	V
Hysteresis width	VTHHYS	VTHCSF - VTHCSN		0.6		V
Clamp voltage at latch mode	VCS2	FB pin : open		8.9		V

Cutoff circuit at overload (FB pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Detection threshold voltage	VTHFB		3.3	3.6	3.9	V

Cutoff circuit at overvoltage (VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Threshold voltage	VTHVCC		26	28	30	V
CS pin charging current	ISOCS2	CS pin = 4V		-1.3		mA

Malfunction-protective circuit at low voltage (VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
ON threshold voltage	V_{CCON}		13.2	15.0	16.8	V
OFF threshold voltage	V_{CCOFF}		8.0	9.0	10.0	V
Hysteresis width	V_{HYS}	V_{CCON} - V_{CCOFF}	4.5	6.0	7.5	V

Output section (OUT pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Low output voltage	V_{OL}	I_{OL} = 100mA		0.5	1.0	V
High output voltage	V_{OH}	I_{OH} = -100mA, V_{CC} = 18V	14.8	16.4		V
Rise time	tr	C(Load) = 1nF		37		ns
Fall time	tf	C(Load) = 1nF		59		ns

High voltage input section (VH pin, VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
VH pin input current	IHrun	VH pin = 450V, Vcc> Vccon	12	25	37	uA
	IHstb	VH pin = 100V, Vcc = 0V		7.0		mA
VCC voltage in latch mode	V_{CCL}	VH pin = 100V		23		V
VCC pin charging current	Ipre1	Vcc = 10V, VH pin = 100V at start-up or protection mode (OCP, OVP)		-6.6	-4.0	mA
	Ipre2	Vcc = 13V, VH pin = 100V at start-up or protection mode (OCP, OVP)		-6.5	-3.5	mA

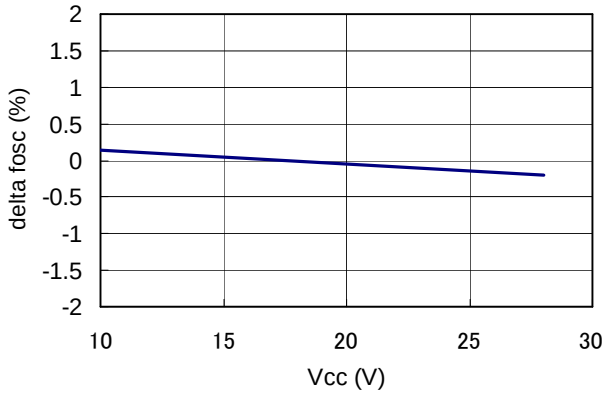
Consumption current (VCC pin)

Item	Symbol	Condition		MIN	TYP	MAX	Unit
Supply current during operation	I_{CCOP1}	Duty cycle = D_{MAX}, FB pin =3V, no load	FA5526/36		1.6	2.4	mA
			FA5527/37		1.5	2.2	
			FA5528/38		1.4	2.0	
	I_{CCOP2}	Duty cycle = 0%, FB pin = 0V			1.6	2.4	mA
Consumption current in latch mode	I_{CCL}	FB pin, CS pin : open			290	400	uA
Zener voltage	Vz	Iz = 2mA			30		V

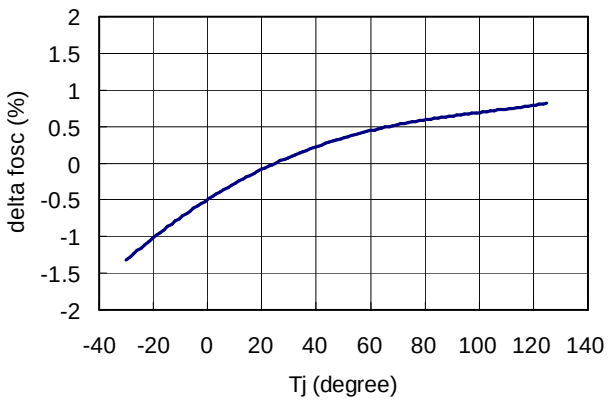
8. Characteristic curves

- Unless otherwise specified, Ta=25℃, Vcc=18V
- In defining a current, “+” represents a sink current and “-” a source current.
- The data stated in this chapter are intended for giving typical IC characteristics and not for guaranteeing performance.

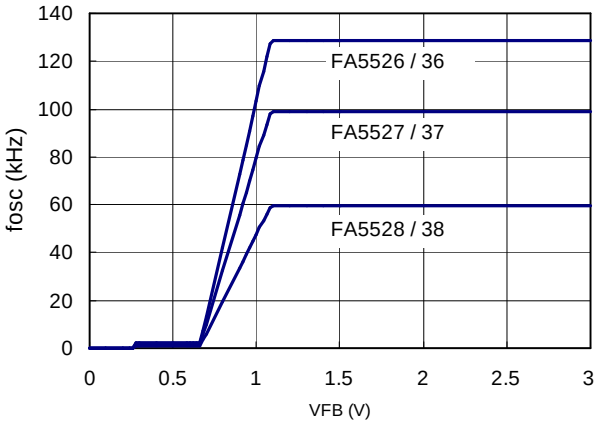
Variation Ratio of Switching Frequency (delta fosc) vs. VCC pin voltage (Vcc)



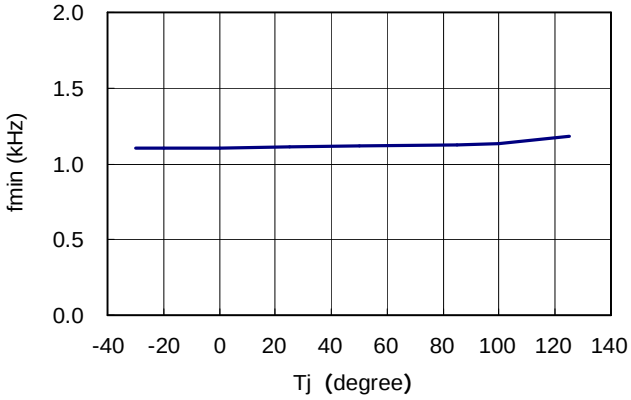
Variation Ratio of Switching Frequency (delta fosc) vs. Junction Temperature (Tj)



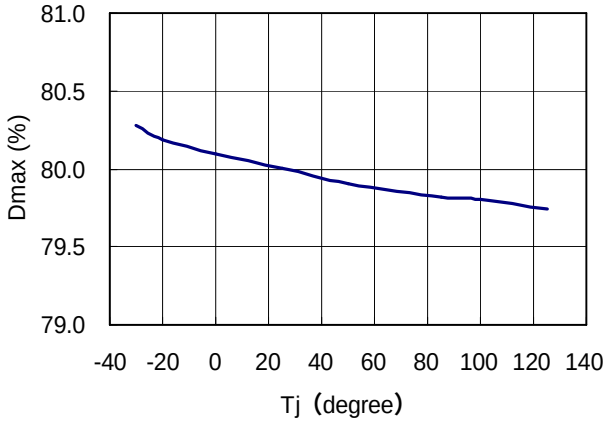
Switching Frequency (fosc) vs. FB pin voltage



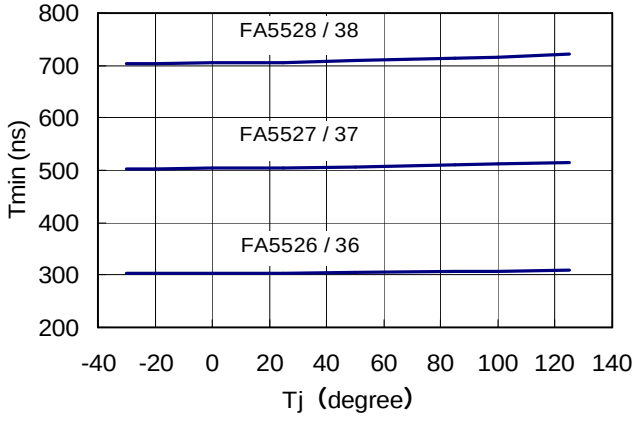
Minimum Switching Frequency (fmin) vs. Junction Temperature (Tj)



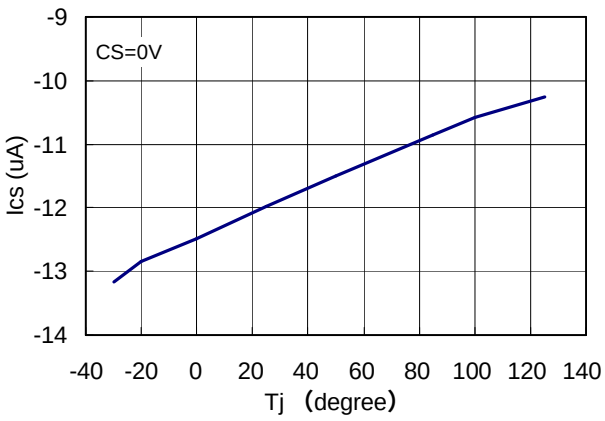
Maximum Duty Cycle (Dmax) vs. Junction Temperature (Tj)



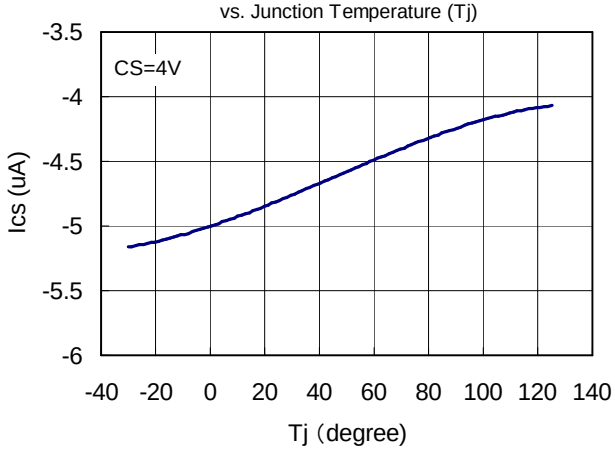
Minimum ON Width (Tmin) vs. Junction Temperature (Tj)



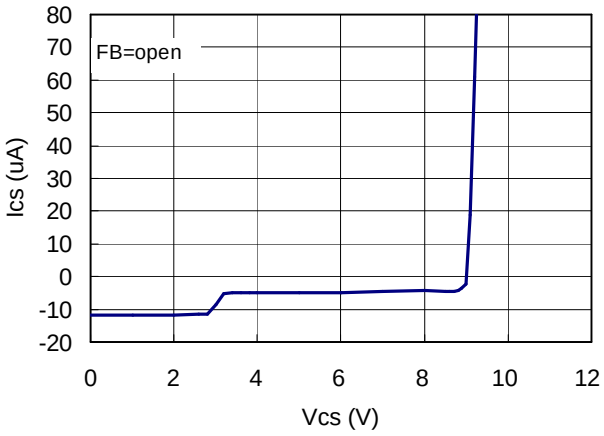
CS pin source current (Ics)
vs. Junction Temperature (Tj)



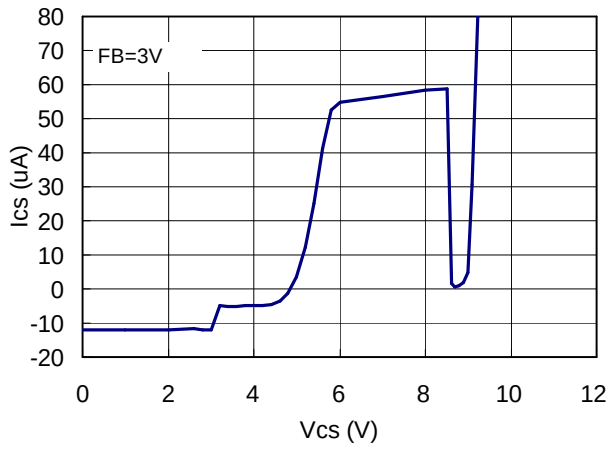
CS pin source current (Ics)
vs. Junction Temperature (Tj)



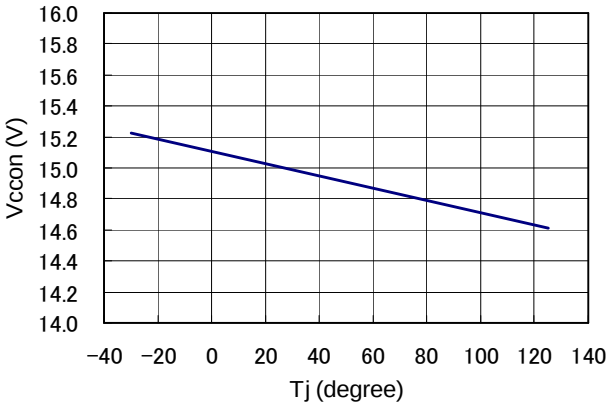
CS pin current (Ics) vs. CS pin voltage (Vcs)



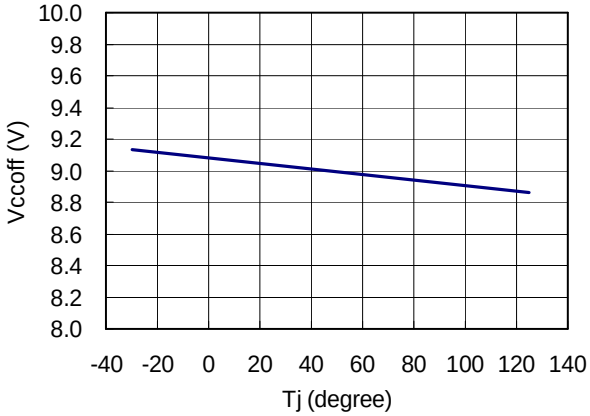
CS pin current (Ics) vs. CS pin voltage (Vcs)



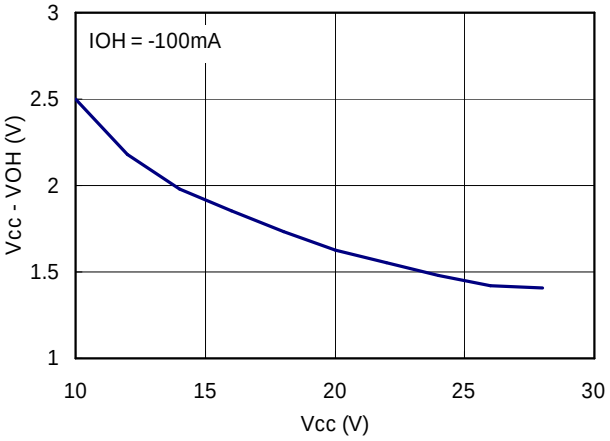
UVLO ON threshold voltage (Vccon)
vs. Junction Temperature (Tj)



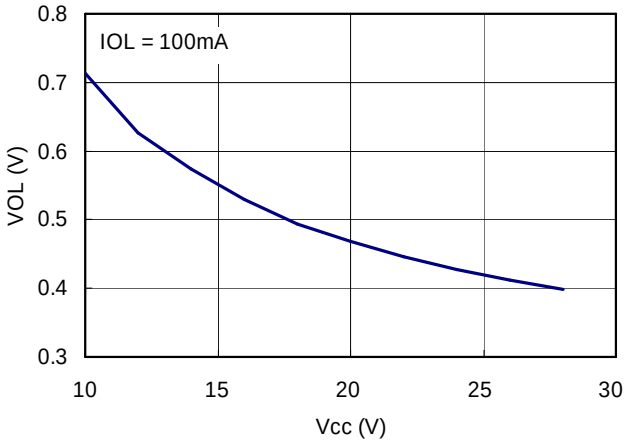
UVLO OFF threshold voltage (Vccoff)
vs. Junction Temperature (Tj)



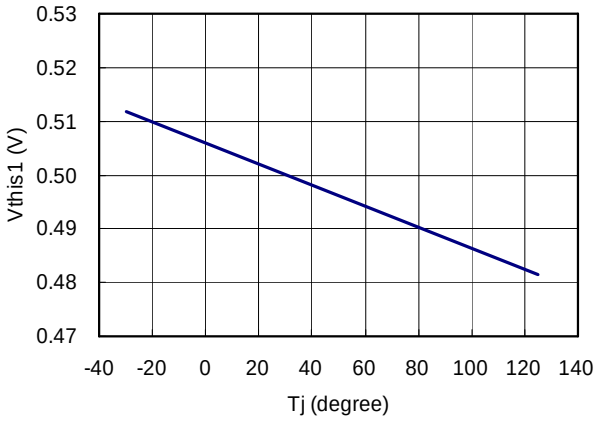
OUT pin High Output Voltage (VOH)
vs. VCC pin Voltage (Vcc)



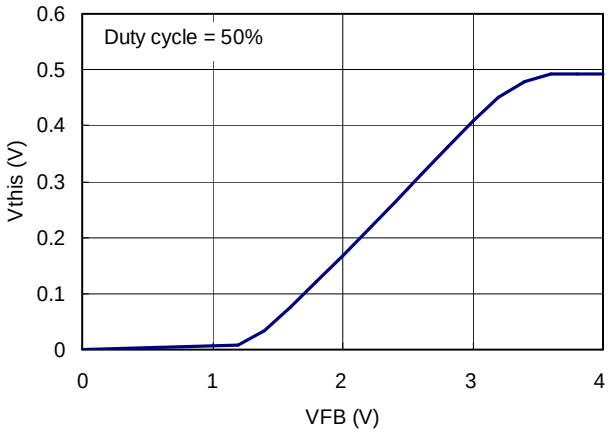
OUT pin Low Output Voltage (VOL)
vs. VCC pin Voltage (Vcc)



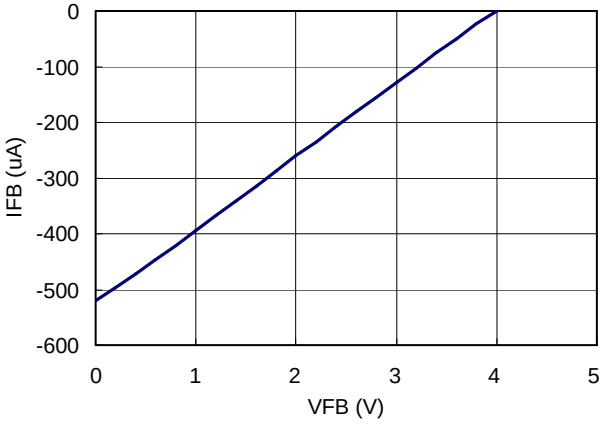
IS pin maximum input threshold volatge(Vthis1)
vs. Junction Temerature (Tj)



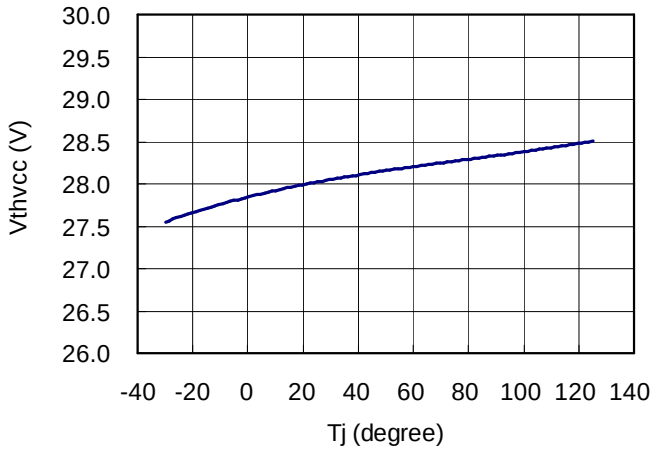
IS pin input threshold voltage (Vthis)
vs. FB pin voltage (VFB)



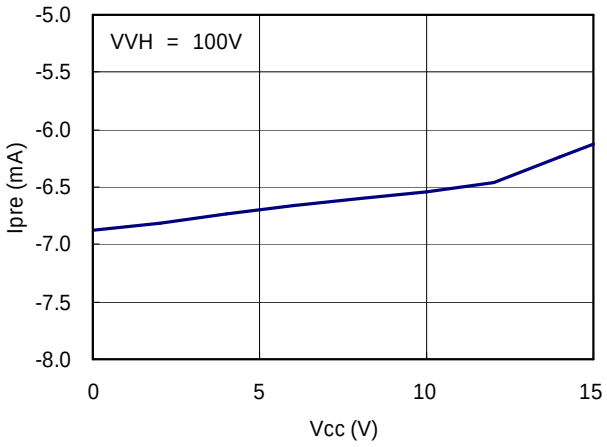
FB pin source current (IFB) vs. FB pin voltage (VFB)



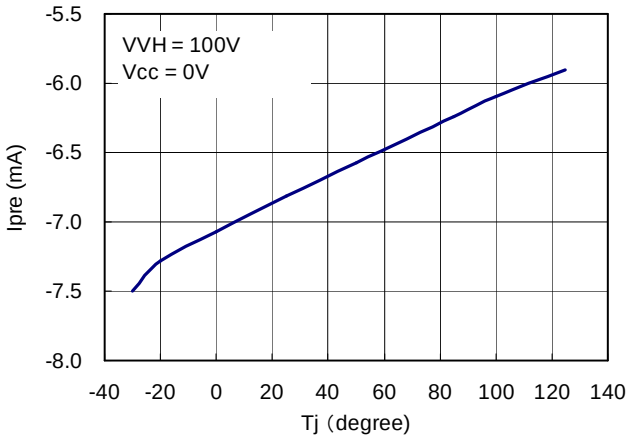
Threshold Voltage of Over-Voltage Protection
(Vthvcc) vs. Junction Temperature (Tj)



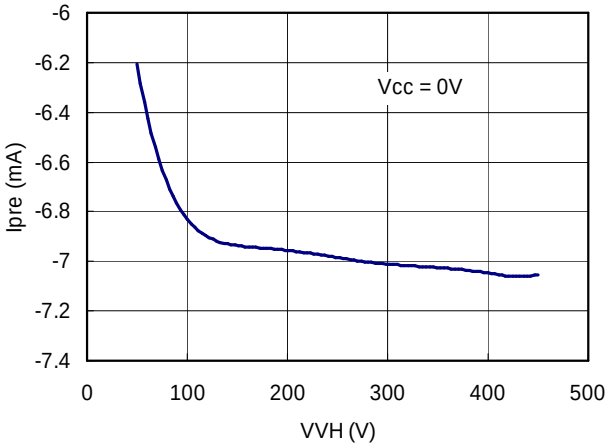
Start-up Circuit VCC pin Source Current (Ipre)
vs. VCC pin voltage (Vcc)



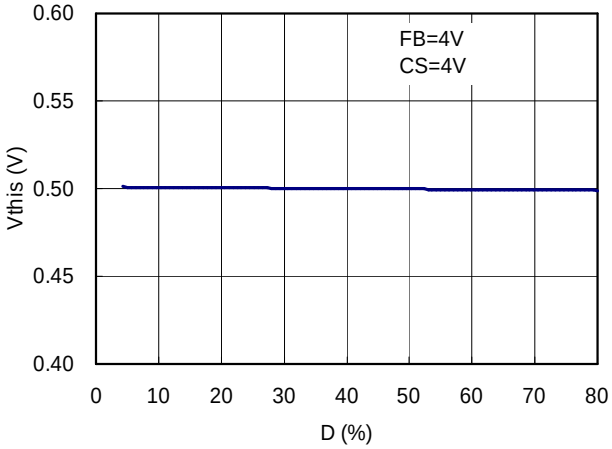
Start-up Circuit VCC pin Source Current (Ipre)
vs. Junction Temperature (Tj)



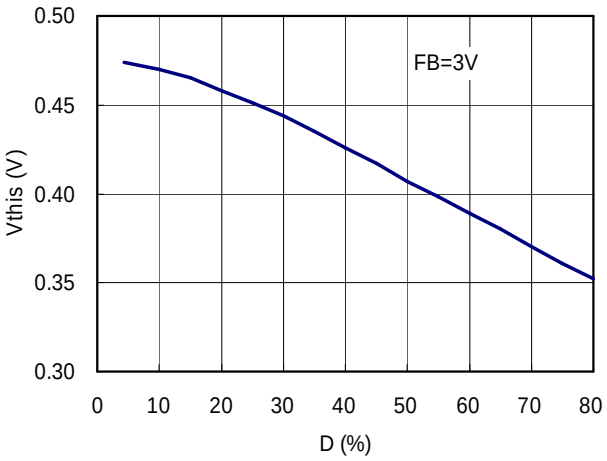
Start-up Circuit VCC pin Source Current
vs. VH pin voltage (VVH)



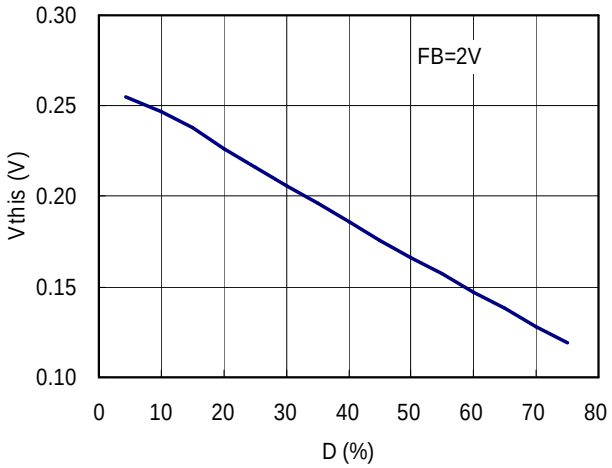
IS pin threshold voltage (Vthis) vs. Duty Cycle
at FB pin = 4V and CS pin = 4V



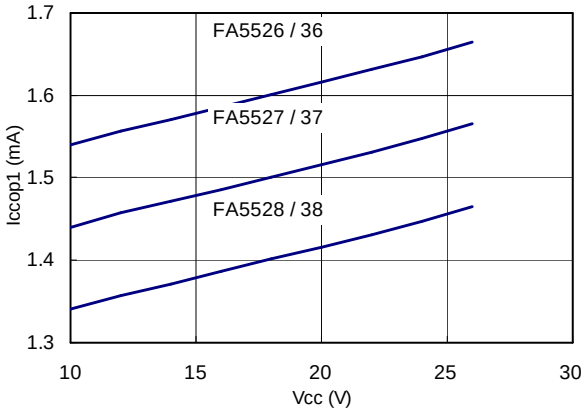
IS pin threshold voltage (Vthis) vs. Duty Cycle(D)
at FB pin = 3V for FA5528/5538



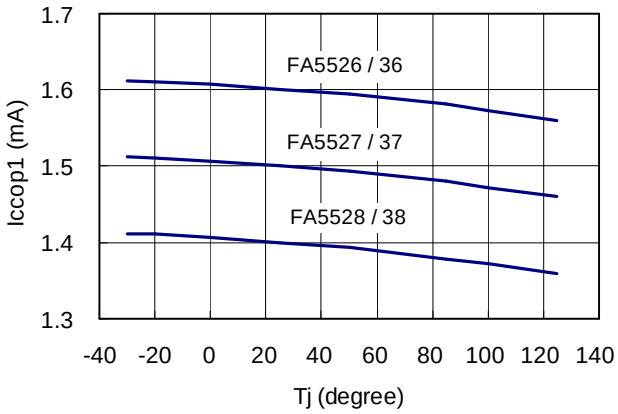
IS pin threshold voltage (Vthis) vs. DutyCycle(D)
at FB pin = 2V for FA5528/5538



Operating Mode Supply Current
vs. VCC pin voltage (Vcc)



Operating Mode Supply Current (Iccop1)
vs. Junction Temperature (Tj)



9. Description of block circuits

(1) Start-up circuit

The FA5526/27/28/36/37/38 has built-in start-up circuits with maximum rated voltage of 500V.

Wiring is shown in **Figs.1** to **3**.

When power is turned on, a current is supplied to the VCC pin from the start-up circuit, charging the capacitor, C2, connected to the VCC pin, increasing its voltage, activating the IC, and the power supply starts operation.

The current supplied to the VCC pin from the VH pin is approximately 6.8mA at Vcc=0V, decreases as Vcc increases and becomes approximately 6.1mA at the start-up voltage. A resistor is connected in series to the VH pin to prevent the IC from being damaged due to surge in AC and other lines.

Fig.1 shows the commonest wiring, connecting the VH pin to half-wave rectified AC input voltage and taking the longest start-up time of the three ways of wiring. When AC input voltage is turned off after the circuit changed to a latch mode due to overload or overvoltage protection, the latch mode can be reset in a relatively short time of several seconds because a current is not supplied from the VH pin.

In **Fig.2**, the VH pin is connected to full-wave rectified AC input voltage, reducing start-up time to approximately half as compared to half-wave rectification circuit shown in **Fig.1**. The latch mode can be reset in a short time same as in **Fig.1** because AC input voltage is cut off.

In **Fig.3**, the VH pin is connected to rectified and smoothed AC input voltage, resulting in the shortest start-up time of the three ways of wiring. In this way of wiring, it takes time for the latch mode to be reset because charged C1 voltage is applied to the VH pin even if the IC have changed to the latch mode. Depending on usage conditions, in general it takes several minutes.

When VCC pin voltage exceeds ON threshold voltage of the low-voltage malfunction-protective circuit and the IC is activated, the start-up circuit is cut off and VH pin input current becomes 25uA (typ.).

When IC enters to the latch mode due to any abnormal condition, the start-up circuit is activated again, the latch condition is maintained and Vcc voltage is held at approximately 23V. Here, FA5526/27/28 enters to the latch mode by overload or over-voltage, but FA5536/37/38 does not enter to the latch mode without an additional external circuit (See “9.-(8)/(9) Overload protection,” “9.-(10)/(11) Over-voltage protection.”).

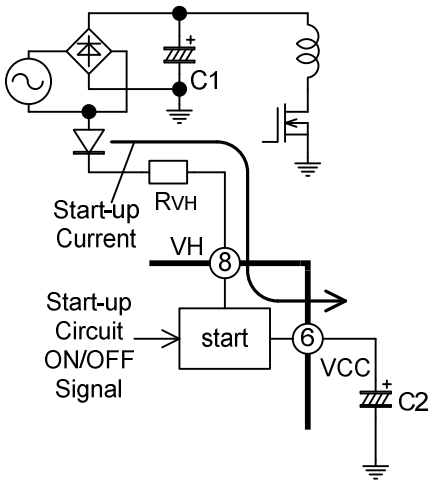


Fig.1 Start-up circuit 1 (half wave)

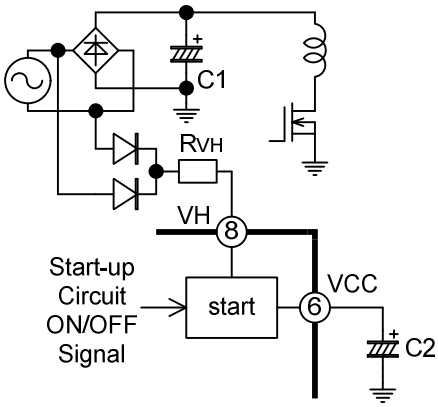
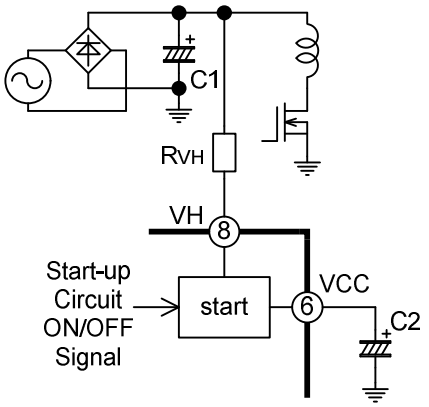


Fig.2 Start-up circuit 2 (full wave)



Note : This circuit makes too long reset time such several minutes for latch mode of OVP, OTP or OLP after power off.

Fig.3 Start-up circuit 3 (DC)

(2) Oscillator

The oscillator determines switching frequency. For steady operation at heavy load, the oscillating frequency is set at 130kHz for FA5526/36, 100kHz for FA5527/37 or 60kHz for FA5528/38 inside the IC.

In addition, the IC has a function to automatically decrease oscillating frequency at light load to reduce standby power dissipation. When FB pin voltage becomes 1.05V or less at light load, the frequency starts decreasing.

At light load, as FB pin voltage drops, the frequency decreases almost linearly to the minimum operating frequency (**Fig.4**). The minimum operating frequency, Fmin, is set at 1.1kHz.

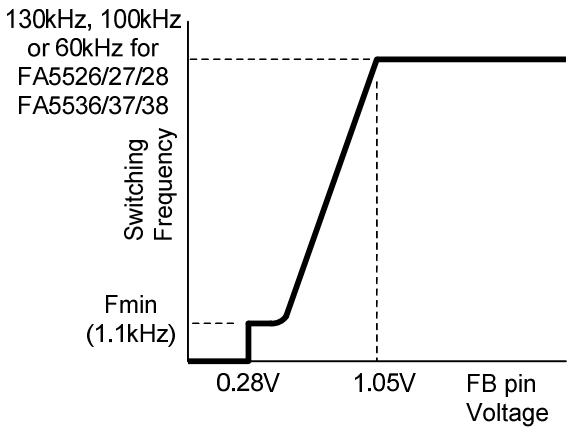


Fig.4 Oscillating frequency

The oscillator generates a trigger signal for determining the switching frequency, a pulse signal for determining the maximum duty cycle and a ramp signal for slope compensation.

(3) Current comparator and PWM latch

FA5526/27/28/36/37/38 have current mode comparators. **Fig.5** shows a block diagram for basic operation and **Fig.6** a timing chart.

A trigger signal is generated by the oscillator and input to the PWM latch (F.F.) as a set signal through a blanking circuit, increasing PMW latch output and also OUT pin voltage.

On the other hand, the current comparator (IS comp.) monitors a MOSFET current and generates a reset signal when OUT pin voltage reaches the threshold voltage. Then, PWM latch (F.F.) output and OUT pin voltage go into low state

The output is controlled through varying IS comparator threshold voltage due to a feedback signal.

As shown in **Fig.7**, FB pin voltage and CS pin voltage are level-shifted and input to the current comparator (IS comp.) as threshold voltage. In addition, the reference voltage of 0.52V is input to the IC to determine IS pin maximum threshold voltage.

The lowest of the three inputs is given a high priority.

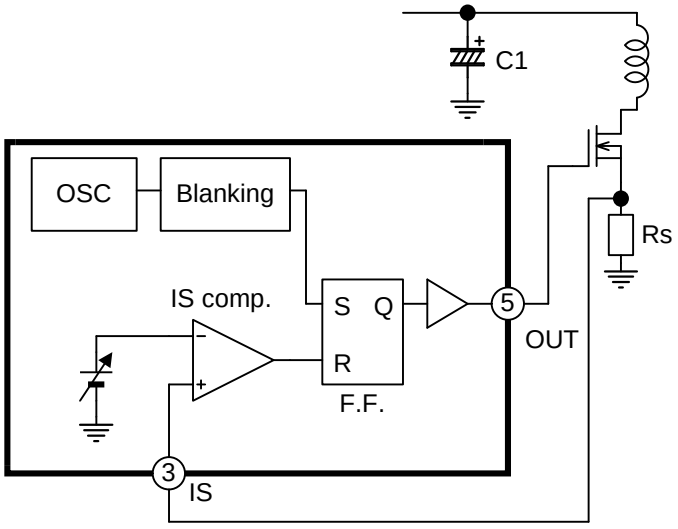


Fig.5 Current-mode basic operation circuit block

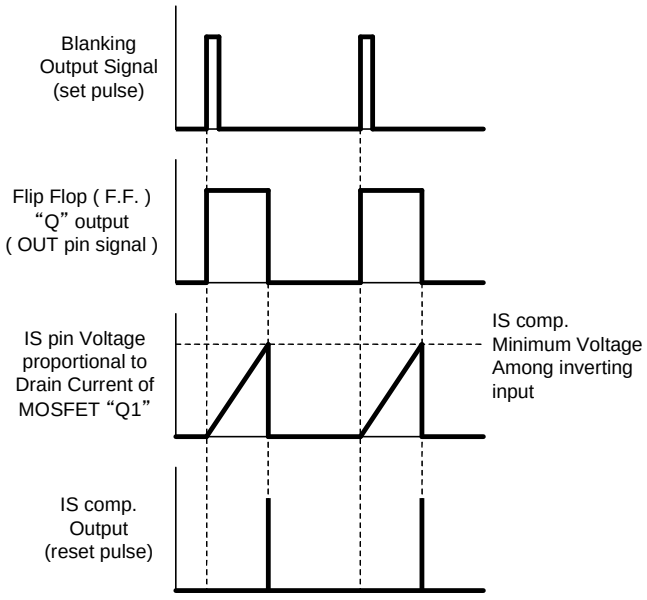


Fig. 6 Timing chart for current-mode basic operation

At start-up, soft start can be realized through gradually increasing the threshold voltage based on CS pin voltage.

At steady operation, the threshold voltage is varied based on FB pin voltage to keep power supply output voltage constant.

In addition, the maximum IS pin threshold voltage as 520mV limits MOSFET over-current when FB pin voltage is very high like 4V by overload etc.

The oscillator generates a pulse to determine the maximum duty cycle of an OUT pulse and the maximum duty cycle is set at 80% (typ.) using this pulse..

For details, refer to “9-(14) Timing chart”.

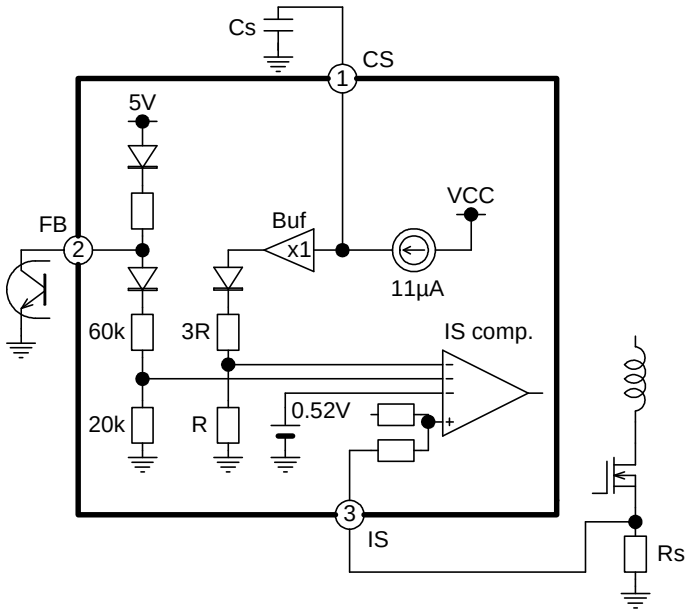


Fig.7 Current comparator

(4) Blanking

When MOSFET turns on, a surge current is generated due to discharge current from the capacitor in the main circuit or gate drive current. If the surge current reaches the IS pin threshold voltage, current comparator output could be inverted and normal pulses would not be generated from the OUT pin.

To avoid this, a blanking function is incorporated into the current comparator. When a trigger signal is input from the oscillator, the blanking circuit outputs a certain-width pulse signal as a PWM latch (F.F.) set signal.

Since the set signal is given a high priority in PWM latch input signals, the output of PWM latch (F.F.) will not be inverted while the set signal is input from the blanking circuit, even if a rest signal is input from the current comparator (IS comp.).

As a result, the IS pin input voltage is ignored for a blanking time (200ns for FA5526/36, 400ns for FA5527/37 and 600ns for FA5528/38) immediately after an output pulse has been generated from the OUT pin and does not respond to a surge current at turn-on.

（See **Fig.8.**）

In general, the blanking circuit eliminates the need for a noise filter at the IS pin.

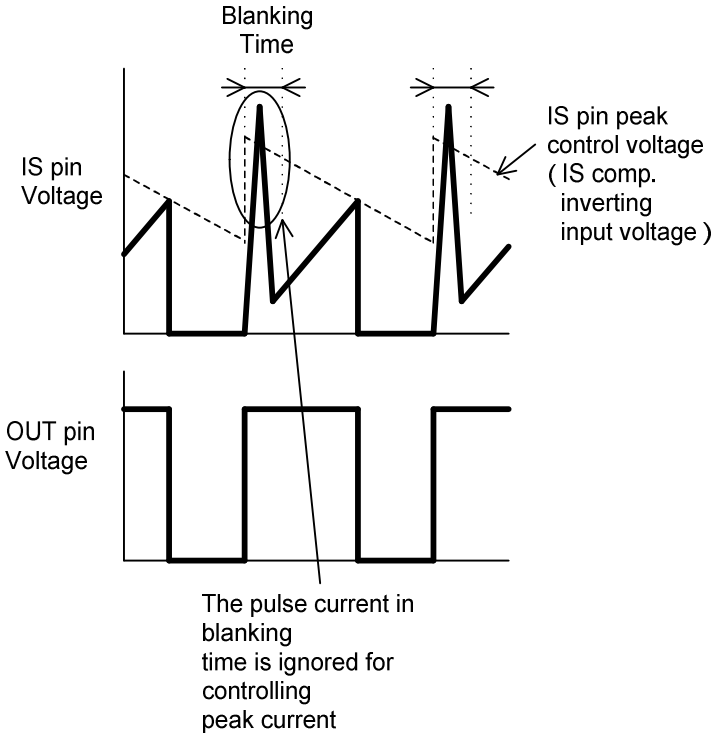


Fig.8 Blanking

(5) Minimum ON pulse width

As described in “(4) Blanking,” the input voltage at the IS pin is ignored during a blanking period right after turn-on. Consequently, the sum of blanking time and output delay time (100ns) is the minimum ON pulse width at the OUT pin of the IC. The minimum ON pulse width for FA5526/36, FA5527/37 and FA5528/38 are 300ns, 500ns and 700ns, respectively.

In addition, a dedicated comparator is incorporated not to generate pulses at no load.

When FB pin voltage is below 0.28V or CS pin voltage is below 0.68V, the output of the comparator is inverted and a clear signal “CLR” is input to the blanking circuit. Then, the blanking circuit will not output a set signal and no set signals will be input to PMW latch (F.F.), keeping the output voltage low.

(See “9-(14) Timing chart.”)

(6) Slope compensation

In the current mode control, subharmonic oscillation may occur at a continuous current mode operation with a duty cycle of 50% or more.

To avoid this, FA5526/36, FA5527/37 and FA5528/38 have built-in slope compensation circuits.

For details of subharmonic oscillation phenomenon and slope compensation effect, see p.32.

As shown in **Fig.9**, slope compensation is achieved by a input of FB pin voltage to the current comparator (IS comp.), which subtracted ramp signal generated from oscillator passing through slope generator.

Therefore, the threshold voltage at the FB pin gradually decreases with time within each switching cycle as shown in **Fig.10** even when voltages at the FB pin and CS pin are constant.

(See “9-(14) Timing chart.”)

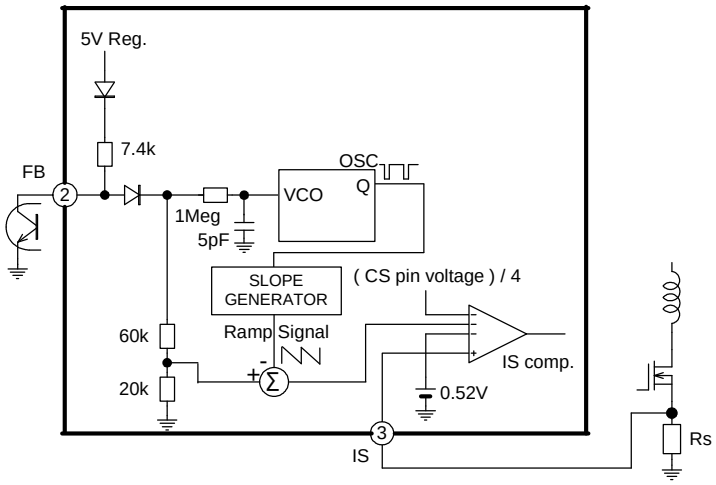


Fig.9 Slope compensation circuit

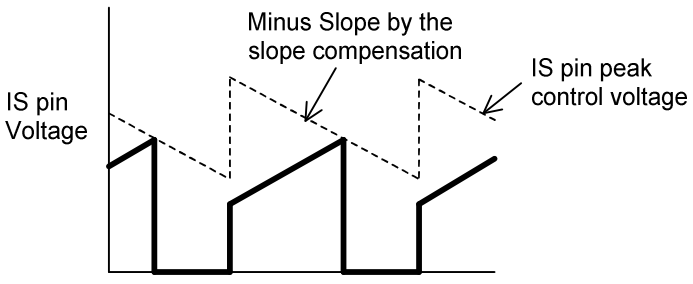


Fig.10 Slope compensation

(7) Soft start circuit

The CS pin is connected to a built-in constant current source. The current for soft start is 11uA.

The capacitor externally connected to the CS pin is charged by the constant current source, gradually increasing CS pin voltage.

MOSFET current gradually increases at start-up because CS pin voltage is input to the current comparator (IS comp.), realizing soft start.

As a guide for soft start time, the time tss taken until CS pin voltage increases from 0V to 3V is given by the following equation.

tss [s] = 0.27 * Cs [uF] (typical value)

Here, Cs is a capacitance connected to CS pin [uF].

In steady operation, CS pin voltage is clamped at approximately 4V by a zener diode in the IC.

The CS pin is provided with a built-in circuit to stop pulses when CS pin voltage is 0.68V or less, same as FB pin.

(See “9-(14) Timing chart.”)

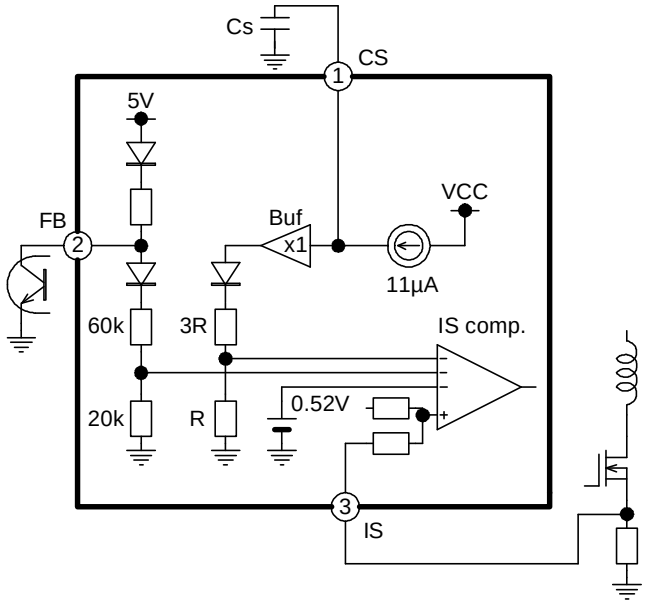


Fig.11 Soft start circuit

(8) Overload protection of FA5526/27/28

FA5526, FA5527 and FA5528 have built-in time-latch type overload protection. **Fig.12** shows its block diagram and **Fig.13** its Timing chart.

In steady operation, FB pin voltage is 3V or less and CS pin voltage is clamped at 4V by a zener diode in the IC.

When power supply voltage drops on account of overload or short-circuit on the load side, FB pin voltage increases. If FB pin voltage exceeds the 3.6V threshold voltage for overload protection, output voltage of a comparator for overload detection (Overload) is inverted and 4V clamp of the CS pin is canceled, increasing CS pin voltage again due to a built-in constant current source. The current supplied from the CS pin becomes 4µA.

If the power supply voltage continues to decrease and CS pin voltage reaches the threshold voltage (8.5V) of the comparator (Latch), the output of the comparator (Latch) is inverted, turning off a 5V circuit in the IC and forcing OUT pin voltage to be low.

This status is the latch mode of the IC. In the latch mode, the start-up circuit resumes operation to supply current to Vcc and to hold the latch mode.

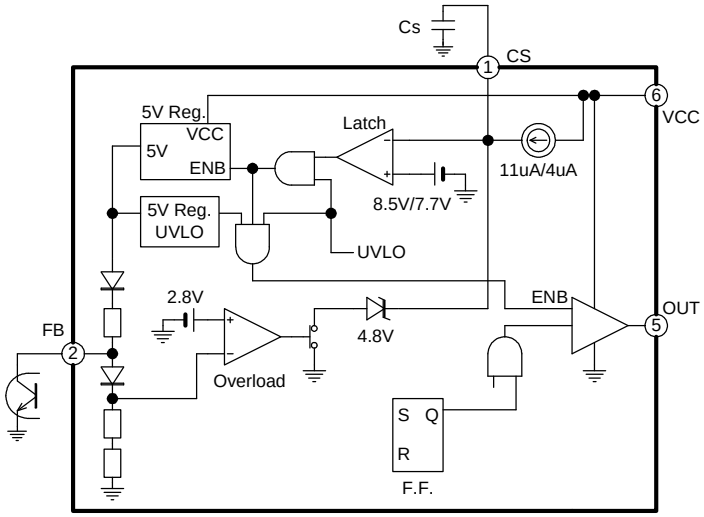


Fig.12 Overload protection circuit

When the output voltage momentarily drops due to abrupt load change and FB pin voltage restores to the voltage at steady state before CS pin voltage reaches 8.5V, the 4V clamp circuit restarts, producing no latch mode.

The latch mode can be reset through cutting off input voltage or through forcibly decreasing CS pin voltage to 7.4V or less.

Cutting off the input voltage decreases VH pin voltage, supplying no current to the VCC pin. Thereafter, the latch mode is reset when Vcc drops below the OFF threshold voltage, 8.0Vmin.

In addition, when CS pin voltage is forcibly decreased, the latch mode comparator is re-inverted and the IC re-starts switching operation.

In the case of typical IC, delay time td (OLP), the time from overload detection to the latch mode, is given by the following equation.

td1 (OLP) [s] = 0.93 * Cs [uF] (typical value)

Here, Cs is a capacitance connected to CS pin [uF].

Delay time td(OLP) is inversely proportional to CS charging current and proportional to the difference between CS pin clamp voltage “4V” at steady condition and latch-mode threshold voltage “8.5V”. Pay attention to variations in delay time resulting from variations in numerical values.

In addition, be aware that when the VH pin is connected after rectification, it takes rather long time, approximately several minutes, before the latch mode is reset.

(See “9-(1) Start-up circuit.”)

(9) Overload protection of FA5536/37/38

FA5536, FA5537 and FA5538 have built-in auto-recovery type overload protection. **Fig.14** shows VCC pin voltage and the drain voltage of power MOSFET “Q1” in the circuit on page 33 at “6A” overload when 90Vac input is applied and **Fig.15** shows same parameters mentioned above at “7A” overload when 264Vac input is applied.

Switching period after the overload occurs and stop period are calculated as follows.

Steady State to Overload : td2 (OLP) [s] = td1 (OLP),

After overload starts : td2 (OLP) [s] = 1.65* Cs [uF],

stop period t (stop) [s] = Cvcc [uF] *

[Vcc(sw/OL) – Vccoff] / (ICCL)

Here,

Vcc(sw/OL) : Vcc in switching period at overload [V]

Vccoff : OFF threshold voltage of U.V.L.O (9V (typ.))

ICCL : Consumption current in latch mode (290uA (typ.))

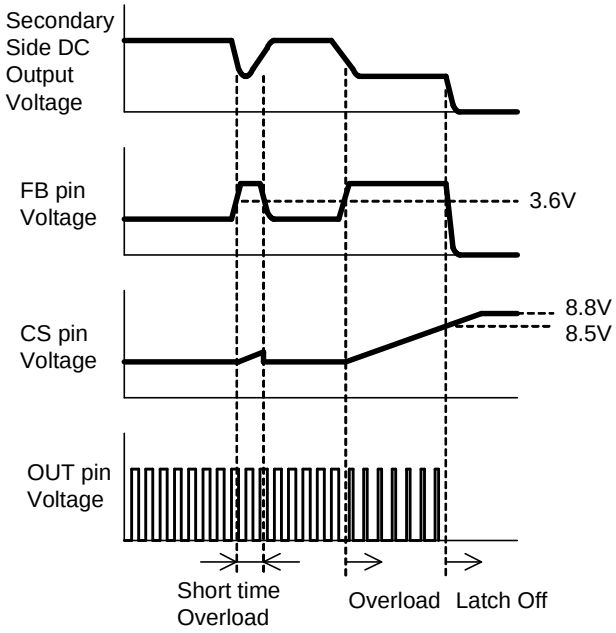


Fig.13 Overload protection timing chart

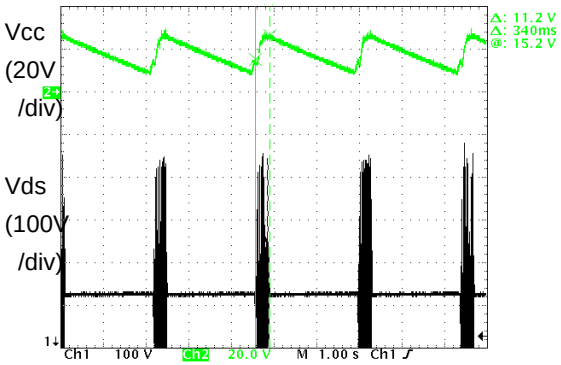


Fig.14 Overload protection waveform of FA5538 as Auto-Recovery (90Vac)

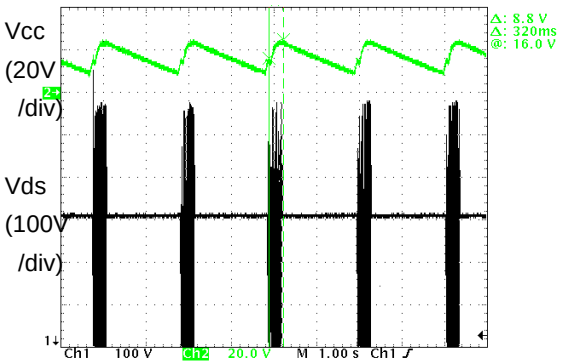


Fig.15 Overload protection waveform of FA5538 as Auto-Recovery (264Vac)

(10) Over-Voltage Protection of FA5526/27/28

FA5526, FA5527 and FA5528 have built-in over-voltage protection circuits to monitor Vcc voltage. **Fig.16** shows its block diagram and **Fig.17** its timing chart.

When VCC voltage increases and exceeds comparator (OVP) reference voltage, 28V, an internal 1.3mA constant current source is tuned on.

Since sink capability of the zener diode which clamps the CS pin at 4V is 55uA, CS pin voltage quickly increases when the 1mA constant current source is turned on. When CS voltage exceeds comparator (Latch) reference voltage, 8.5V, the IC changes to the latch mode.

The delay time td (OVP), the time from over-voltage detection to the latch mode, is given as follows.

td (OVP) [ms] = 2.85 * Cs [uF] (typical value)
Here, Cs is a capacitance connected to CS pin [uF].

In the latch mode, an internal power supply source, 5V "Reg" circuit, is turned off and OUT pin voltage is held to be low., and the current form the CS pin changes to 5μA.

The latch mode can be reset through decreasing Vcc voltage due to cutting off of input voltage or through forcibly decreasing CS pin voltage to 7.4V or less. Moreover, pay attention to the relationship between wiring at the VH pin and reset time in the latch mode.
(See "9-(1) Start-up circuit.")

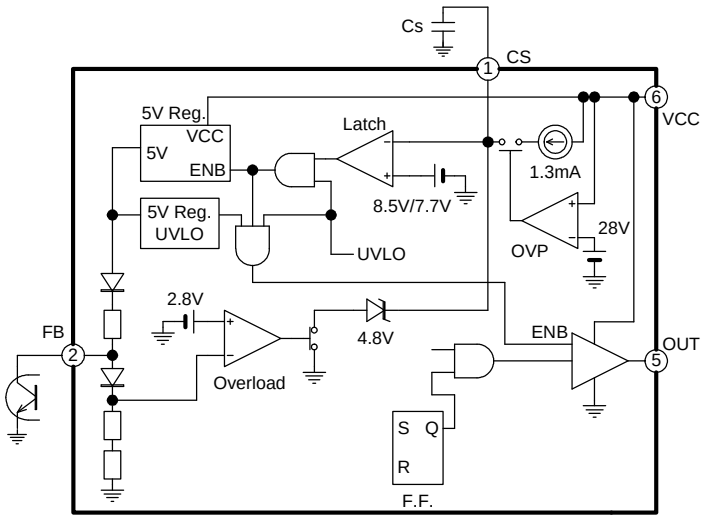


Fig.16 Over Voltage protection circuit (only for FA5526 / 5527 / 5528)

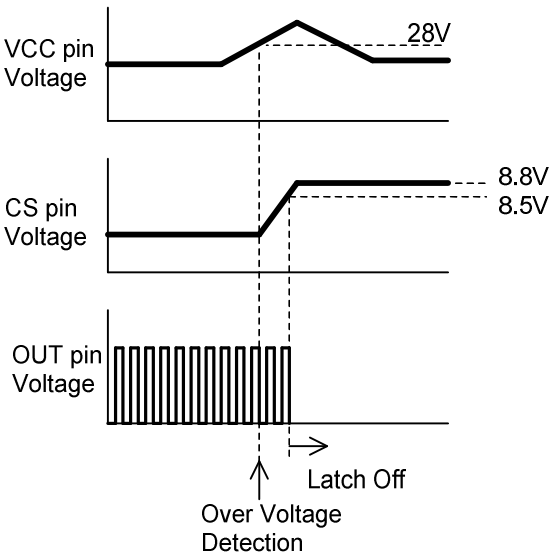


Fig.17 Over-Voltage protection timing chart (only for FA5526 / 5527 / 5528)

(11) Over-Voltage Protection of FA5536/37/38

FA5536, FA5537 and FA5538 have built-in over-voltage protection (OVP) circuits to monitor Vcc voltage similar to FA5526/27/28.

However, the OVP of FA5536/37/38 is **Auto-Recovery mode**.

Therefore, when you need the OVP as latch mode, the additional external circuit is necessary as mentioned on page 28 to 29 (See "10-(4)").

(12) Under-Voltage Lock-Out circuit

The IC has a built-in undervoltage lockout circuit to prevent malfunction when Vcc voltage drops. When Vcc voltage increases from 0V, the IC starts operation at Vcc = 15V (typ.). As the supply voltage decreases, the IC stops operation at Vcc = 9V(typ.).

When the undervoltage lockout circuits operates and the IC stops operation, OUT pin and CS pin voltage are forced to be low, resetting soft start, and overload and overvoltage timer latch protection.

(13) Output circuit

The output circuit consists of push-pull configuration, capable of directly driving a MOSFET. The maximum peak currents at the OUT pin are 0.25A for source current and 0.5A for sink current.

If the IC stops operation when the under-voltage lockout circuit operates or in the latch mode, OUT pin voltage is forced to be low to shut down the MOSFET.

(14) Timing chart

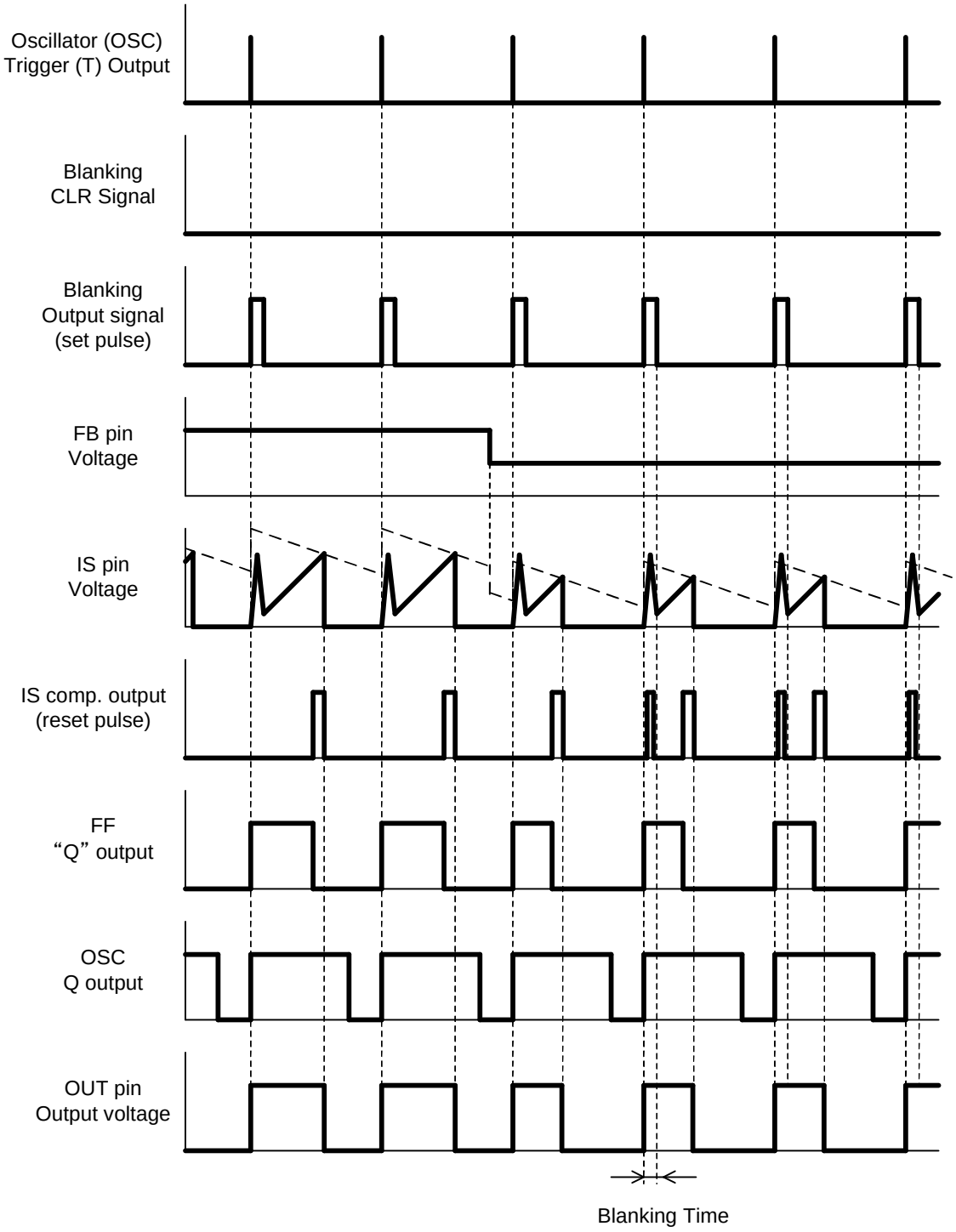


Fig.18 Timing chart at steady operation

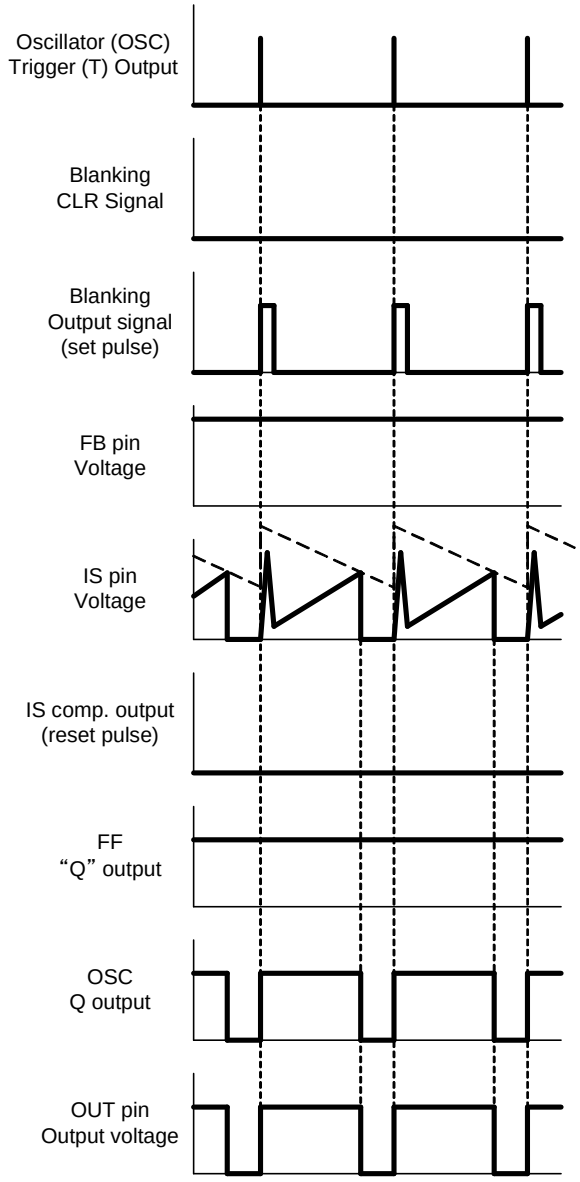


Fig.19 Timing chart at maximum duty cycle operation

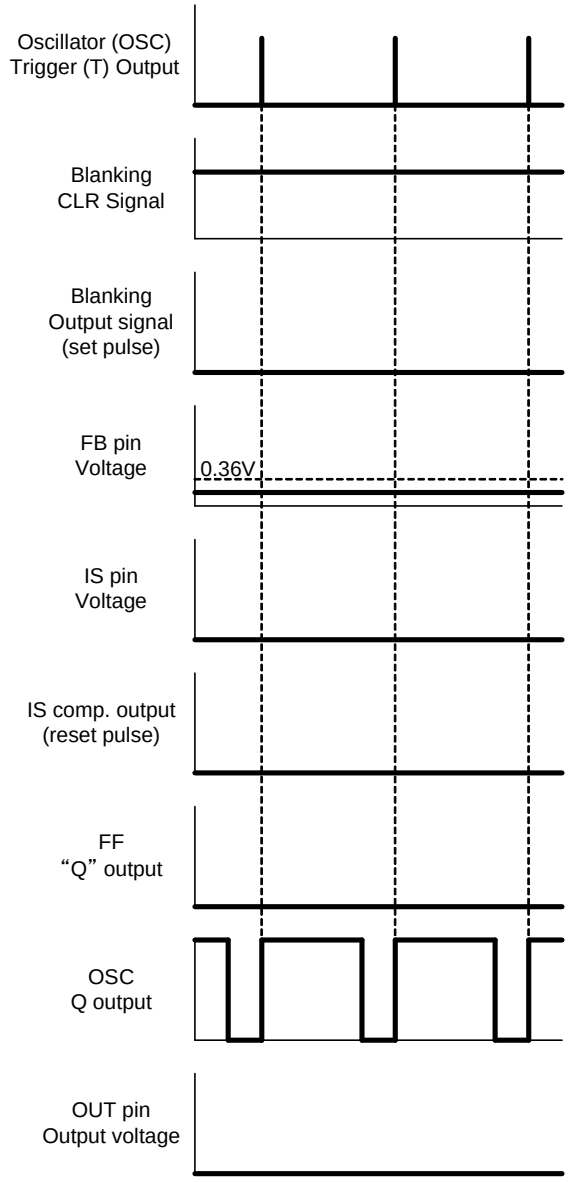


Fig.20 Timing chart at FB pin < 0.36V

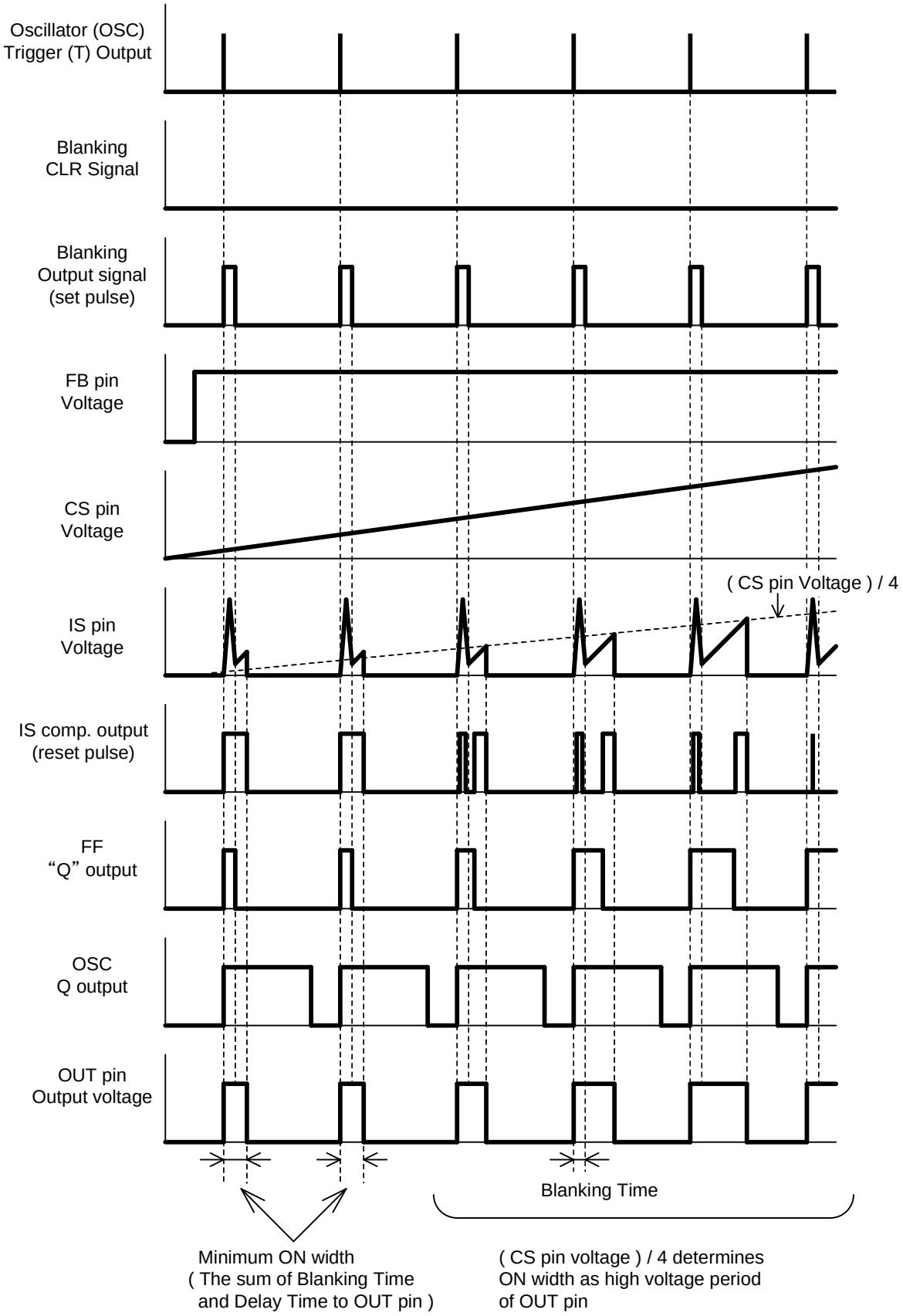


Fig.21 Timing chart at start-up (soft start)

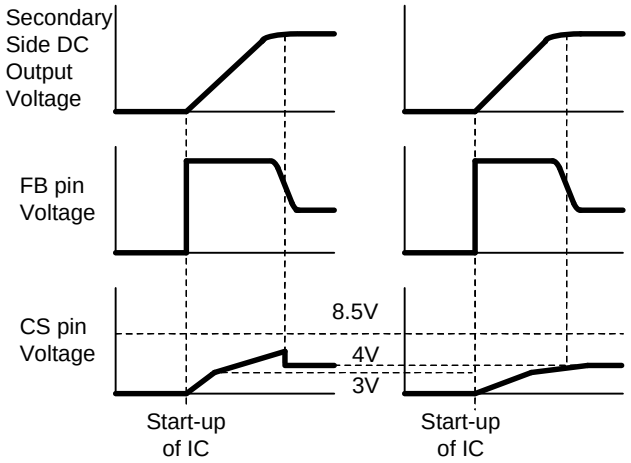
10. Design advice

(1) Start-up and stop

To properly start up and stop the power supply, optimum values shall be set for capacitors connected to the CS pin and VCC pin.

(1-1) At start-up (1)

It takes certain time until the output voltage reaches to the set voltage after the IC has been activated. During this period, FB pin voltage reaches its maximum voltage and the 4V clamp circuit does not operate. As a result, with proper CS pin capacitance and proper start-up, CS pin voltage waveform during start-up will be as shown in **Fig.22**.



a) After CS pin exceeds 4V, FB pin voltage drops.　　b) Before CS pin exceeds 4V, FB pin voltage drops.

Fig.22　CS pin voltage waveform at start-up (1)

(normal start)

On the other hand, when CS pin capacitance is too small, CS pin voltage may reach the threshold voltage of the latch mode as shown in **Fig.23** before the output voltage increases to the set value. The IC changes into a latch mode and the power supply cannot start properly. In cases like this, increase CS pin capacitance.

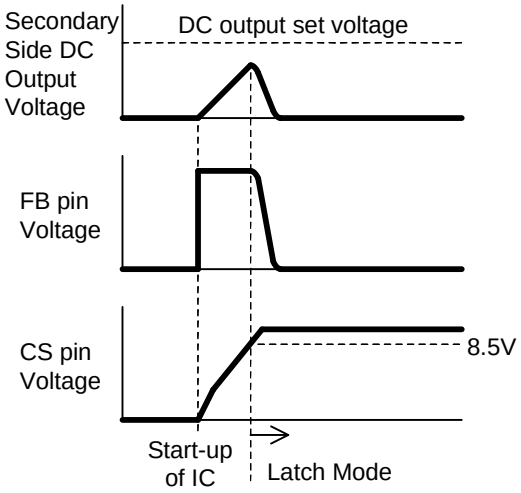


Fig.23　CS pin voltage waveform at start-up (2)

（when the power supply can not start up）

(1-2) At start-up (2)

Fig.24 shows Vcc voltage at start-up when proper capacitance is connected.

When input power is turned on, the VCC capacitor is charged by the current supplied from the start-up circuit and its voltage increases. Then, when Vcc reaches the ON threshold voltage, the IC starts operation. In steady operation, the IC operates at the voltage supplied from an auxiliary winding. Right after IC start-up, however, Vcc drops until the auxiliary voltage increases sufficiently. Determine the capacitance connected to VCC pin so that Vcc does not drop to the OFF threshold voltage in any condition.

We recommend that you choose the capacitance connected to VCC pin so that the bottom of Vcc becomes larger than 11V as the result of typical experiment.

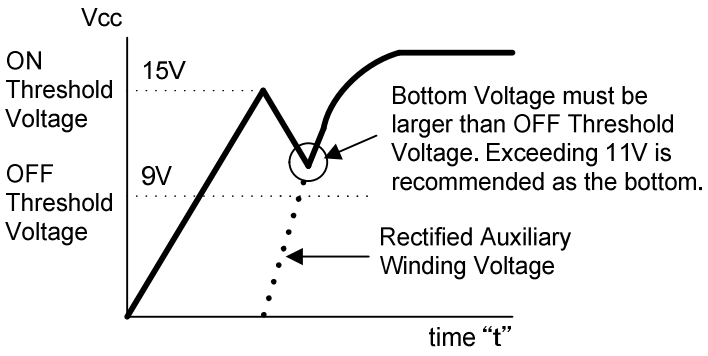


Fig.24　Vcc waveform at start-up (1)

（at normal start-up）

When Vcc capacitance is too small, Vcc drops to the OFF threshold voltage as shown in **Fig.25** before the auxiliary winding voltage increases sufficiently. In this case, Vcc repeatedly goes up and down between the ON and OFF threshold voltages, and the power supply can not start up.

(1-3) At stopping

When the power supply is turned off by shutdown of input voltage, output voltage remains low for certain period of time before the IC stops operation.

During this period, FB pin voltage increases and the CS pin clamp circuit is cancelled because output voltage remains low. As a result, CS pin voltage increases as shown in **Fig.26**.

CS pin voltage shall not reach the threshold voltage of the latch mode. As shown in **Fig.27**, if CS pin voltage reaches the threshold voltage, the latch mode is held for a period of time until Vcc capacitor voltage drops to OFF threshold voltage. As a result, the power supply cannot be re-started even if input voltage is turned on again.

In such a case, the following measures shall be taken:

- Reduce the time taken until the IC stops operation after the output voltage has dropped through reducing Vcc capacitance.
- Suppress CS pin voltage rise through increasing CS pin capacitance.

(2) Hold time of Vcc

In some cases, VCC pin capacitance shall be increased to hold Vcc above the OFF threshold voltage at abrupt load change after the power supply has started up.

However, when VCC pin capacitance becomes larger, start-up time gets longer.

In such a case, the circuit shown in **Fig.28** is effective.

Reducing C2 shortens start-up time, and hold time can be kept long because power is supplied via C4 after start-up.

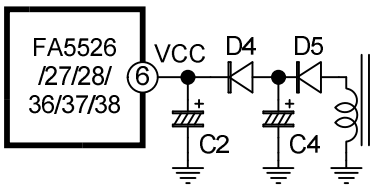


Fig.28 Vcc circuit

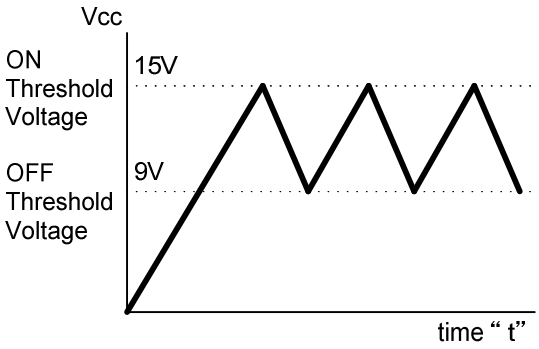


Fig.25 Vcc waveform at start-up (2)
（when the power supply can not start up）

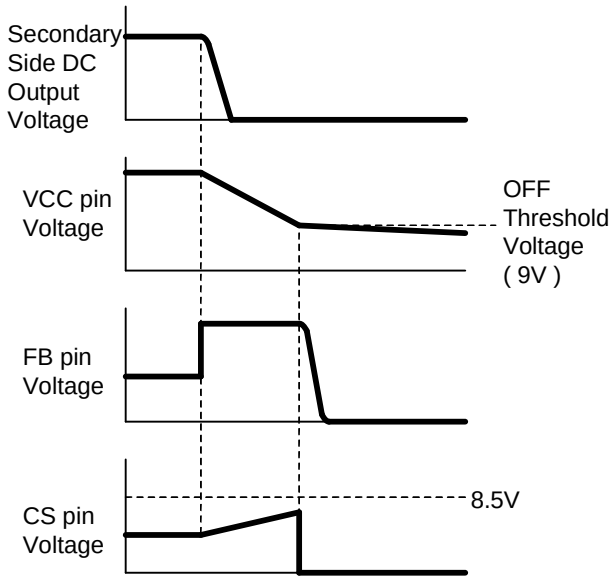


Fig.26 Waveform at stopping (1)

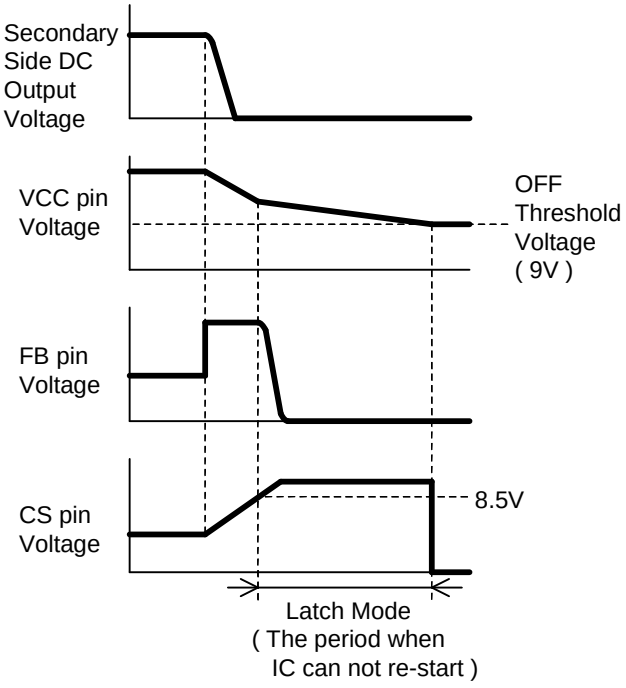


Fig.27 Waveform at stopping (2)

(3) Protection using CS pin for FA5526/27/28

In steady operation, the CS pin voltage is clamped by a 4V zener diode. Externally forcing CS pin voltage to increase to the threshold voltage, 8.5V, for the latch mode allows the IC to stop its operation for protection.

In this case, a current of more than the sink capacity of 4V zener diode, 84uA, shall be applied to the CS pin.

Set the input current to the CS pin at 1mA or less as a guide.

The following shows examples of overvoltage protection at an arbitrary voltage using the CS pin.

(3-1) Overvoltage detection on the secondary side

Fig.29 shows an example of an overload detection circuit on the secondary side to change the IC into the latch mode.

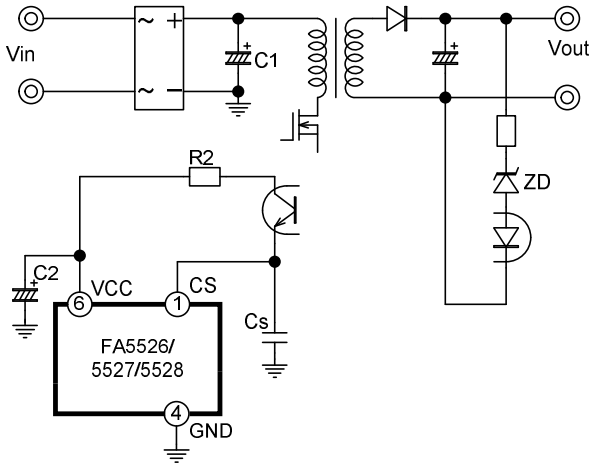


Fig.29 Over Voltage protection (1) for FA5526/27/28

(3-2) Detection of Vcc (1)

Fig.30 shows a circuit where the IC is stopped in the latch mode upon detecting Vcc overvoltage. In this case, Vcc voltage is latched at approximately ZD+8.5V.

Use a ZD whose voltage is larger than the ON threshold voltage of the low-voltage malfunction preventive circuit. Otherwise, the IC cannot start.

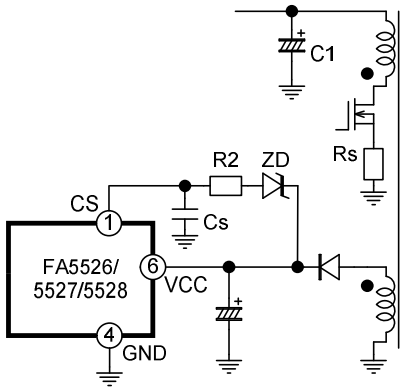


Fig.30 Over Voltage protection (2) for FA5526/27/28

(3-3) Detection of Vcc (2)

Fig.31 shows another circuit to detect Vcc overvoltage. In this case, Vcc voltage is latched approximately at ZD voltage.

Use a ZD whose voltage is larger than the ON threshold voltage of the low-voltage malfunction preventive circuit. Otherwise, the IC cannot start.

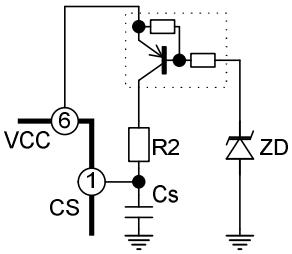


Fig.31 Over Voltage protection (3) for FA5526/27/28

(4) Protection using CS pin for FA5536/37/38

FA5536/37/38 does not include any latch function.

Therefore, the external latch circuit is necessary for Over-Voltage Protection as latch mode. **Fig.32** shows the OVP latch circuit by primary side detection at VCC pin and **Fig.33** shows the OVP latch circuit by secondary side detection through a optocoupler “PC”.

When CS pin voltage is pulled down below 0.68V (typ.), the switching is shut-down. Once the NPN transistor “Q2” and “Q3” turn-on when the diode “ZD1” or optocoupler “PC” supplies the current to resistor “R1” by detection of Over-Voltage, PNP transistor “Q1” turns-on and “Q2” and “Q3” are maintained in ON-State.

Then, CS pin voltage is maintained at low level until the current of a diode ZD2 is cut VCC pin voltage decreases below OFF threshold (9V) .

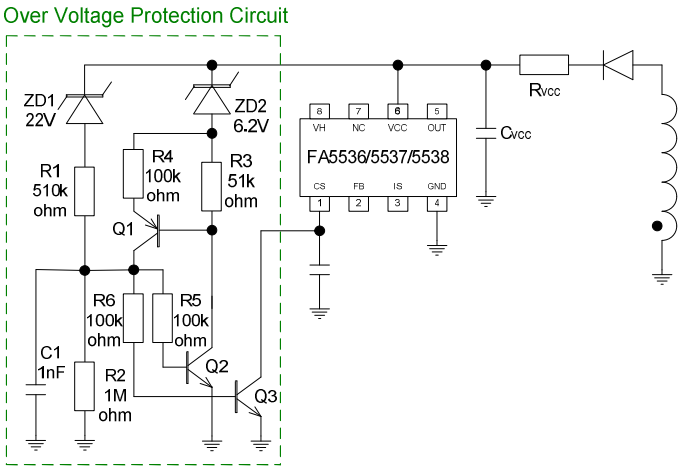


Fig.32 Over Voltage protection (1) for FA5536/37/38

(5) When not using an overload protection function

As shown in **Fig.34**, connect a resistor R3 of 18k ohm between FB pin and GND.

As a result, FB pin voltage does not increase to the threshold voltage for overload protection and the IC does not change to the latch mode even at overload.

In this case, the latch protection for over-voltage is also available.

(6) Correction of overload detection current (Line Conversation)

If the power supply output becomes overload, the current of the MOSFET is limited by the maximum threshold voltage of the IS pin and power supply voltage drops. If the state continues as it is, an overload protection function operates to stop the IC in the latch mode. For details of an overload protection function, see “9-(8) Overload protection function.”

When the overload protection operates, the output current of the power supply varies depending on the input voltage; and the higher the input voltage is, the larger the output current.

In such a case, connect R4 between the current detection resistor Rs and IS pin, and add a correction resistor R5 as shown in **Fig.35**. The typical resistance of R5 is several hundreds of k ohm to several Meg ohm. Note that the above correction slightly decreases the value of overload current limit to stop the IC in the latch mode even if input voltage is low.

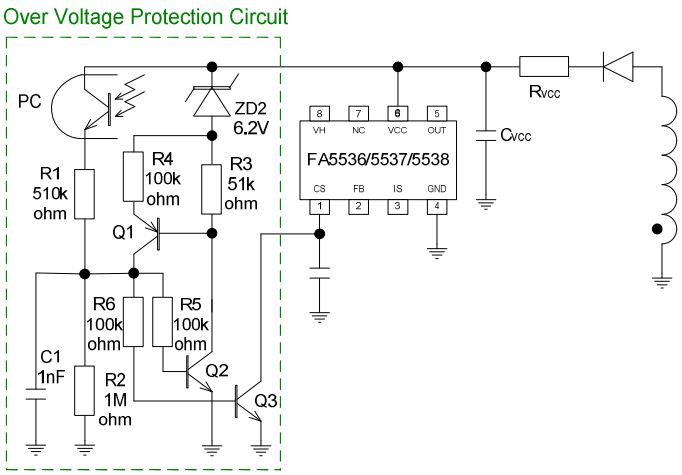


Fig.33 Over Voltage protection (2) for FA5536/37/38

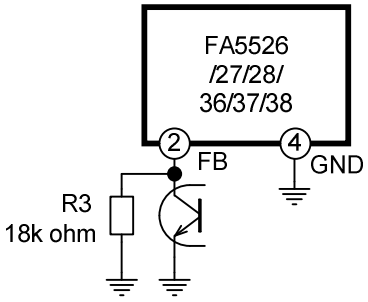


Fig.34 When not using overload protection

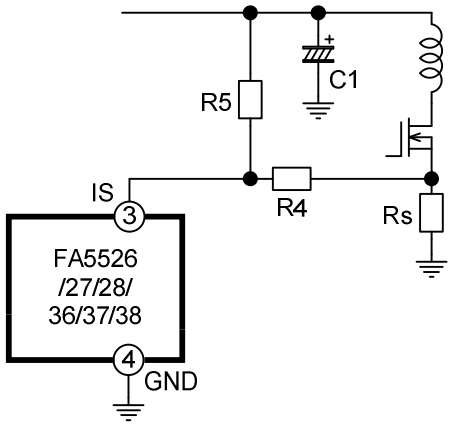


Fig.35 Correction of overload detection current
(Line Conversation)

(7) Improvement of input power at light load

This IC is provided with a function to lower switching frequency at light load in order to reduce power dissipation. However, depending on the circuit used, switching frequency cannot be sufficiently reduced, leading to insufficient reduction of power dissipation at light load.
In such a case, connect R6 between the auxiliary winding and the IS pin as shown in **Fig.36**. When R4 is 1k ohm, R6 is several hundreds of k ohm to 1Meg ohm. The smaller the R6 is, the lower the switching frequency at light load.

However, negative voltage is applied to the IS pin due to R6 for some time while MOSFET is ON. Be aware that the negative voltage shall not be lower than absolute maximum rationg,-0.3V.

In addition, when switching frequency is set too low at light load, transformer or other apparatus may produce noise.

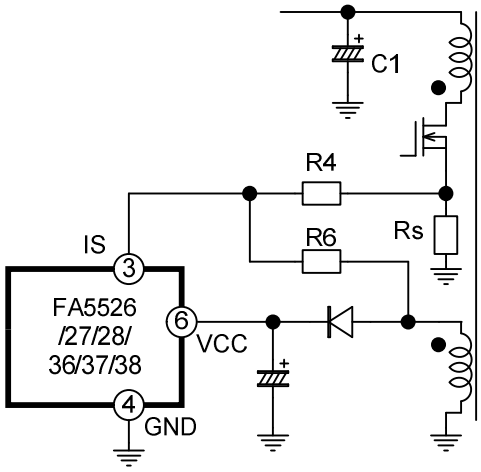


Fig.36 Input power improvement circuit at light load

(8) Prevention of malfunction caused by noise

This IC is an analog IC, and noise applied to anyone of the pins may cause malfunction. If malfunction is detected, use the IC through referring to the following description and fully checking a power supply unit.

In addition, arrange the capacitors connected to pins as close to the IC as possible and take great care of wiring, for effective noise suppression.

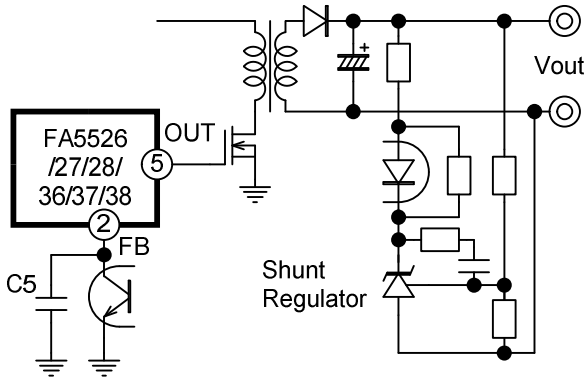


Fig.37 Prevention of malfunction caused by noise (FB pin)

(8-1) FB pin

The FB pin sets the threshold voltage of the current comparator. Any noise applied to the FB pin may disturb output pulses. Usually the capacitor C5 is connected as shown in **Fig.37** to suppress noise.

(8-2) IS pin

As described in “9.-(4) Blanking,” this IC has a blanking function, and malfunction caused by a surge current produced at turn-on of the MOSFET is hard to occur.

A malfunction, however, may occur when a surge current is excessively large or when any noise is externally applied at other than turn-off.

In such a case, add a CR filter to the IS pin as shown in **Fig.38**.

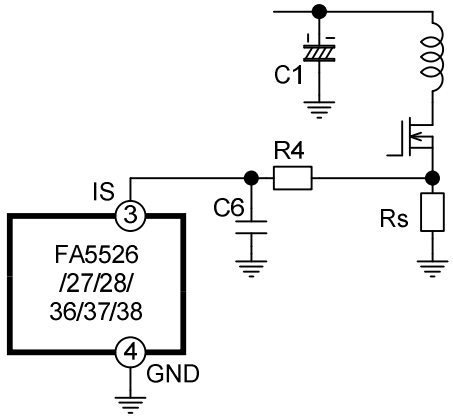


Fig.38 Prevention of malfunction caused by noise (IS pin)

(8-3) VCC pin

Relatively large noise may occur at the VCC pin because a large current flows from the VCC pin at the instant of driving the MOSFET. If noise is excessively large, a malfunction may occur of the IC. Pay full attention to capacitance and characteristics of the capacitor between the VCC pin and GND to reduce noise as much as possible.

(9) Over Temperature Protection as latch mode for FA5526 / 27 / 28

Over Temperature Protection as latch mode can be achieved by the circuit shown in **Fig.39** for FA5526/27/28.

Here, a diode D1 connected to separated line from VCC pin, because the start-up time of IC may become too long when the circuit including a thermistor is connected to VCC pin of IC directly.

Please note that the circuit shown in **Fig. 39** can not be used for FA5536/37/38, because FA5536/37/38 does not include any latch function.

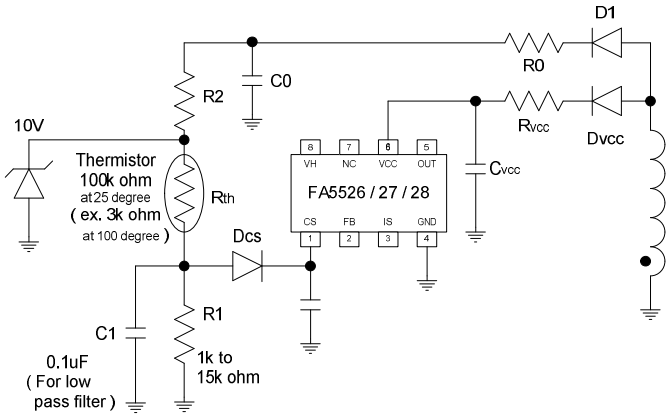


Fig. 39 Over Temperature Protection by Latch Mode for FA5526 / 5527 /5528

Note : OTP Latch by FA5536 / 5537 / 5538 can not be achieved by above circuit. FA5536 / 5537 / 5538 may need very complicated circuit for OTP latch.

(10) Prevention of malfunction caused by negative voltage applied to pins

When a large negative voltage is applied to a pin, a parasitic element in the IC may operate and cause a malfunction. Be sure that voltage applied to a pin shall not be -0.3V or less.

Voltage oscillation generated at turn-off of the MOSFET may be applied to the OUT pin via the parasitic capacitance of the MOSFET, resulting in the negative voltage applied to the OUT pin.

In such a case, connect a Shottky diode between each pin and GND. Forward voltage of the Shottky diode can suppress negative voltage at each pin. Use a Shottky diode with low forward voltage.

Fig.40 shows an example of a circuit with a Shottky diode connected to the OUT pin.

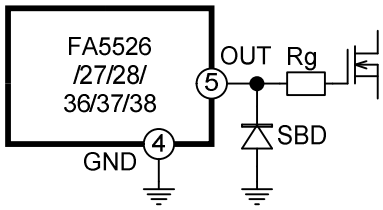


Fig.40 Negative voltage prevention circuit

(11) Gate circuit configuration

A resistor is generally inserted between the gate terminal of the MOSFET and the OUT pin of the IC for adjustment of switching speed, suppression of voltage oscillation at the gate terminal and other purposes.

Sometimes, the drive currents for turning-on and -off must independently determined.

In such a case, connect the gate terminal of the MOSFET and OUT pin of the IC as shown in **Fig.41** or **Fig.42**.

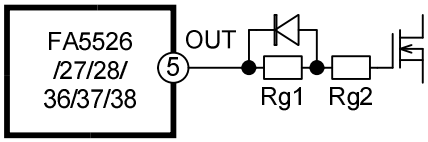


Fig.41 Gate circuit (1)

In **Fig.41**, the driving current is limited by Rg1 + Rg2 at turn-on and by only Rg2 at turn-off

In **Fig.42** the driving current is limited by only RG1 at turn-on and by parallel-connected Rg1 and Rg2 at turn-off.

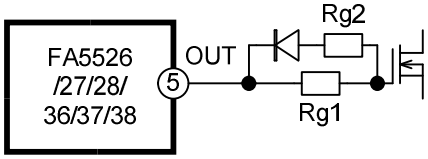


Fig.42 Gate circuit (2)

(12) Loss calculation

IC loss shall be determined to use the IC within its rating. Since it is hard to directly measure IC loss, an example of calculating approximate IC loss is given below.

Total IC loss, Pd, is obtained by the following equation:

$$Pd = Vcc * (Iccop1 + Qg * f) + V_{VH} * IHrun$$

Where Vcc is the supply voltage to the IC, Iccop1 is consumption current of the IC, Qg is total gate charge of the MOSFET, f is switching frequency, V_{VH} is VH pin voltage and IHrun is a current flowing into the VH pin when the IC operates.

This equation gives an approximate value of Pd, which is a little greater than the actual loss. Take into consideration variation and temperature characteristics of each value

(Example)

When the VH pin is connected to half-wave rectification waveform at power supply of 264Vac, the average VH pin voltage is approximately 119V.

Under above condition, let us suppose Vcc = 18V and Qg = 80nC at Tj = 25 degree.

When using FA5528 or FA5538, according to the specifications IHrun = 25uA = 0.025mA (typ.), Iccop1 = 1.4mA (typ.) and f = 60kHz = 0.06MHz (typ.).

Thus, typical IC loss Pd:

$$Pd = 18V * (1.4mA + 80nC * 0.06MHz) + 119V * 0.025mA$$
$$= 115mW (typ.)$$

(Reference)
Sub-harmonic oscillation and slope compensation

In a peak-value-control current mode, when the converter operates in an inductor-current continuous mode and at duty cycle of 50% or more, the current may oscillate at an integral multiple of switching frequency. This oscillation is called subharmonic oscillation.

Fig. 43 shows an example of inductor current waveform when a subharmonic oscillation occurs.

It is found that ON and OFF periods vary while the peak value of an inductor current, switching cycle and current slopes during ON and OFF periods remain unchanged.

The harmonic oscillation may increase ripple voltage contained in the output voltage or cause an unusual noise.

The subharmonic oscillation can be prevented by giving a certain gradient to the threshold of the peak current as shown in **Fig. 44**. This is called slope compensation.

Generally, the gradient of slope compensation required for preventing a subharmonic oscillation is given by the following relational expression:

$$Kc > \frac{Ld - Lu}{2}$$

Here,

Lu : Gradient of an inductor current during the ON period

Ld : Gradient of an inductor current during the OFF period

Kc : Gradient of slope compensation

The above parameters are shown in **Fig.45**.

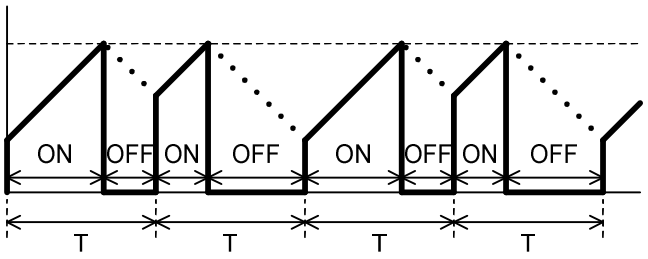


Fig.43 Inductor current without slope compensation

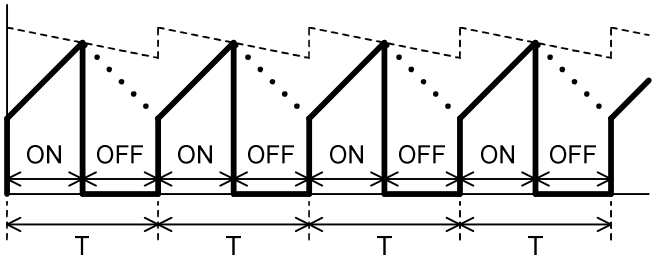


Fig.44 Inductor current with slope compensation

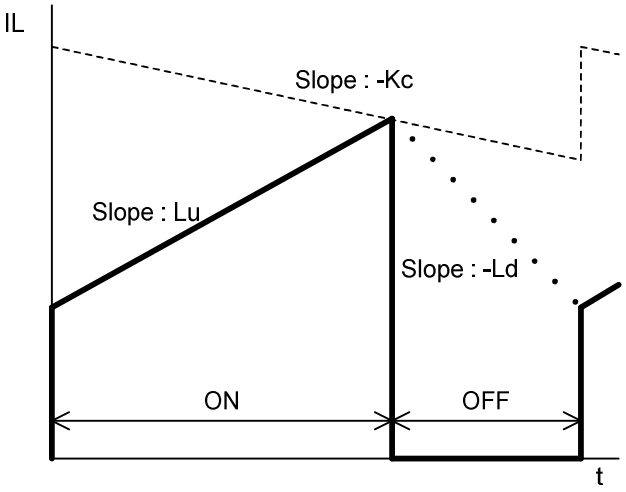
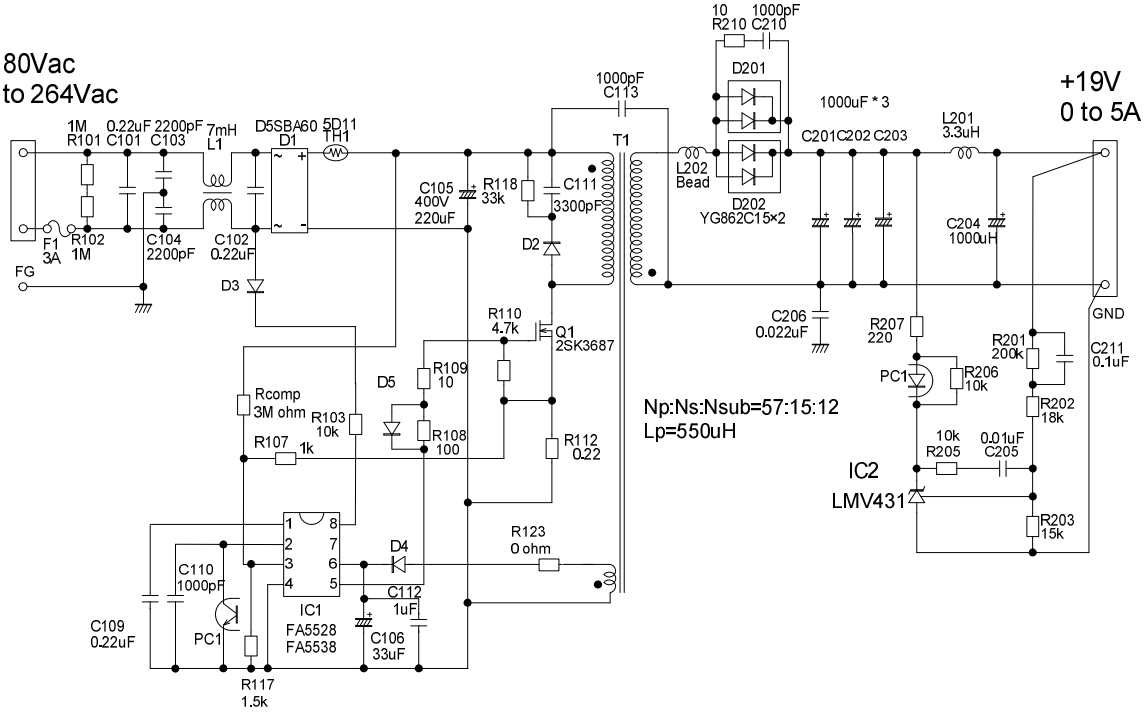


Fig.45 Inductor current without slope compensation

11. Example of an application circuit

The following circuit is common to both of **FA5528** and **FA5538**. FA5526/27/28/36/37/38 can be used for same topology
except the protection circuit and the transformer design which depends on switching frequency.



Note :

The example of an application circuit is intended to be used only for reference and not to guarantee performance or characteristics.