Fuji Switching Power Supply Control IC

Green mode Quasi-resonant IC

FA5640/41/42/43/44/48

Application Note

April 2012
Fuji Electric Co., Ltd.

Caution

1. The contents of this note (Product Specification, Characteristics, Data, Materials, and Structure etc.) were prepared in April 2012.
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   - Traffic signal equipment - Gas leak detector and gas shutoff equipment
   - Disaster prevention/Security equipment - Various equipment for the safety.

6. Products described in this note shall not be used in the following equipments that require extremely high reliability:
   - Space equipment - Aircraft equipment - Atomic energy control equipment
   - Undersea communication equipment - Medical equipment.

7. When reprinting or copying all or a part of this note, our company's acceptance in writing shall be obtained.

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Contents

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- The contents of this note will subject to change without notice due to improvement.
- The application examples or the components constants in this note are shown to help your design, and variation of components and service conditions are not taken into account. In using these components, a design with due consideration for these conditions shall be conducted.

1. Overview

FA5640 series are a quasi-resonant type switching power supply control IC with excellent stand-by characteristics. Though it is a small package with 8 pins, it has a lot of functions and enables to decrease external parts. Therefore it is possible to realize a small size and a high cost-performance power supply.

2. Features

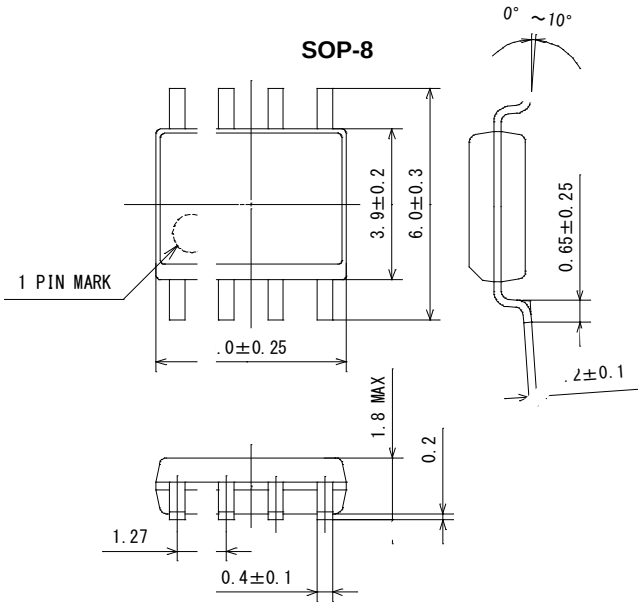
- A quasi-resonant type switching power supply
- A power supply with excellent standby characteristics
- Low power consumption achieved by integrated startup circuit
- Low current consumption, During operation: 0.85 mA
- Control of number of bottom skips by on-off width detection
- Burst operation function under light load
- Built-in drive circuit directly connectable to a power MOSFET, Output current: 0.5 A (sink)/0.25 A (source)
- Built-in overload protection function
- Built-in latch protection function based on overvoltage detection on the secondary side
- Maximum input threshold voltage of IS pin and threshold voltage of stopping on-pulse are compensated by detecting high-line voltage.
- Built-in under voltage lock out function, ON threshold voltage: 14 V and 10 V
- Package: SOP-8

Function list by types

Type	Overload protection	ON threshold voltage	Operation compensation	Minimum switching frequency	Delay time of restart	IS pin one shot latch function	Changing of overload protection levels due to external signal detection	Change point from 1st bottom to 2nd bottom
FA5640	Auto recovery	14V	Yes	No	25us	No	Yes	110kHz
FA5641	Auto recovery	14V	Yes	**25kHz**	**7.6us**	No	Yes	110kHz
FA5542	Auto recovery	**10V**	**No**	No	25us	No	Yes	110kHz
FA5543	Auto recovery	14V	Yes	**25kHz**	25us	**Yes**	**No**	110kHz
FA5544	**Timer latch**	14V	Yes	No	25us	No	Yes	110kHz
FA5548	Auto recovery	14V	Yes	No	12.5us	No	**No**	**260kHz (speeding up)**

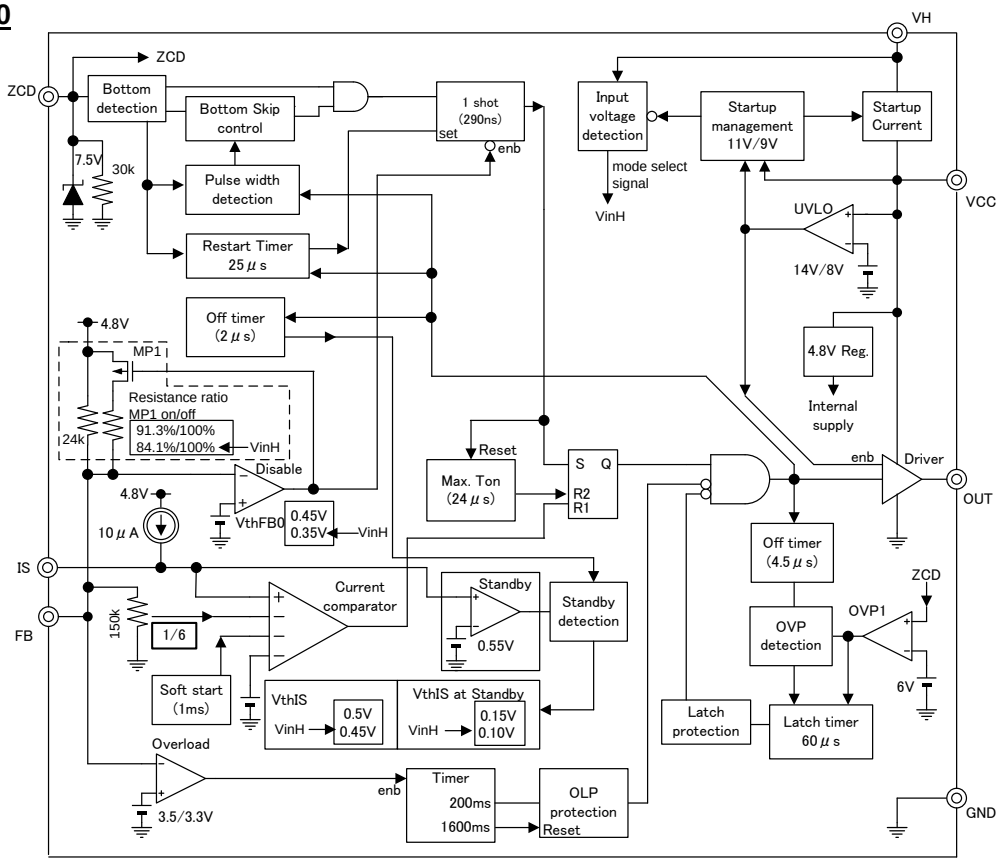
3. Outline drawings

SOP-8



4. Block diagram

FA5640



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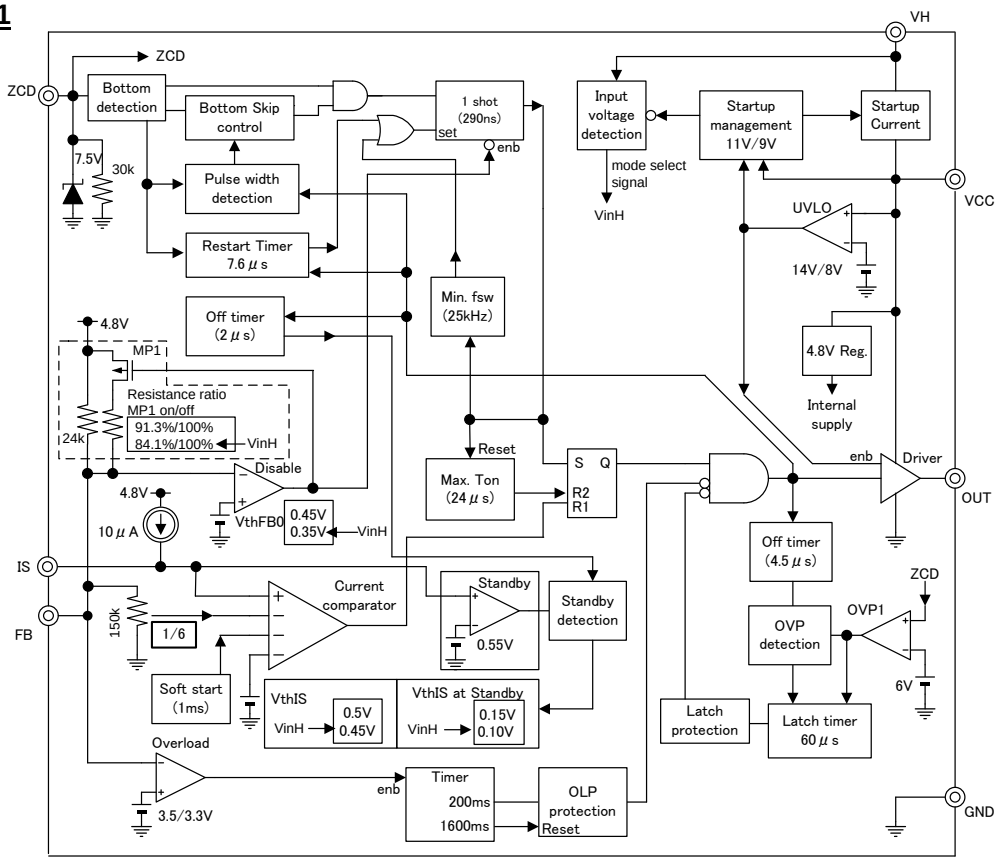

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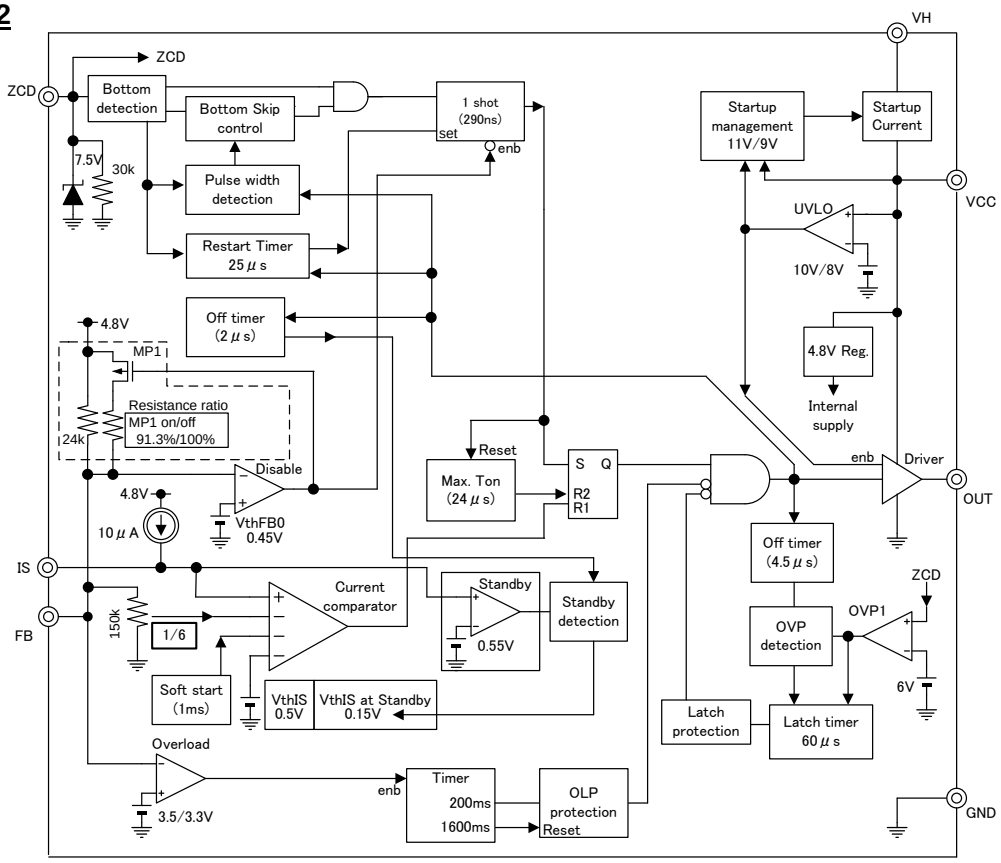

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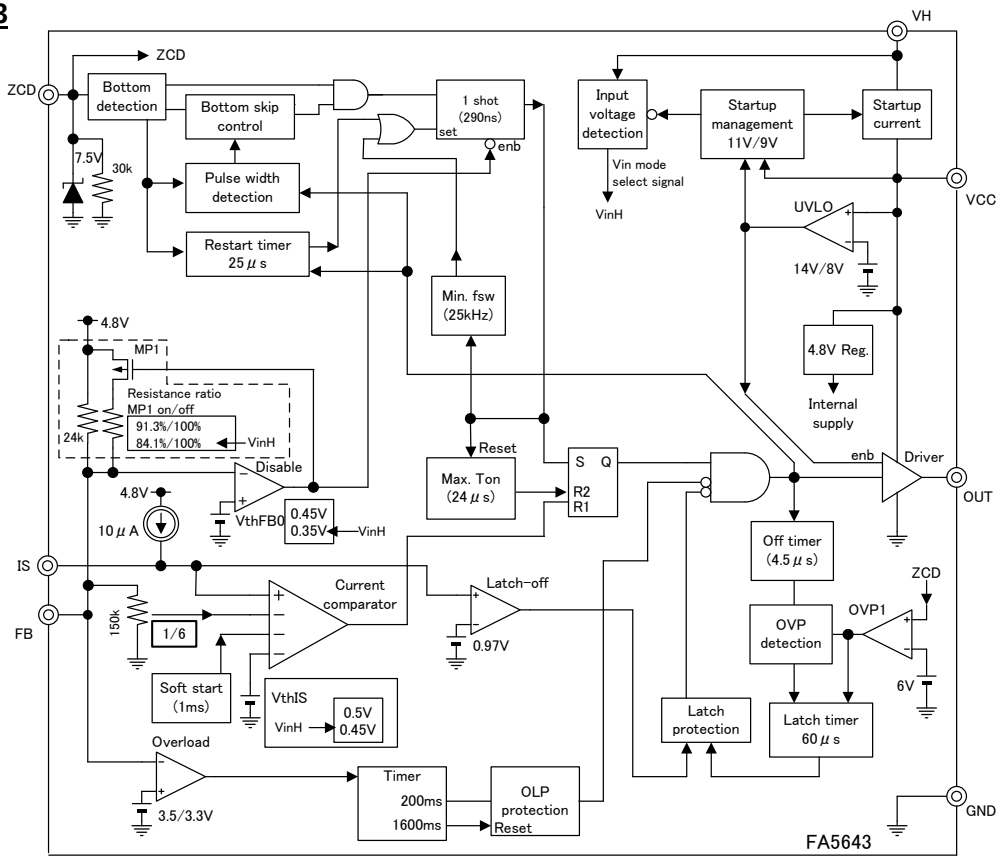

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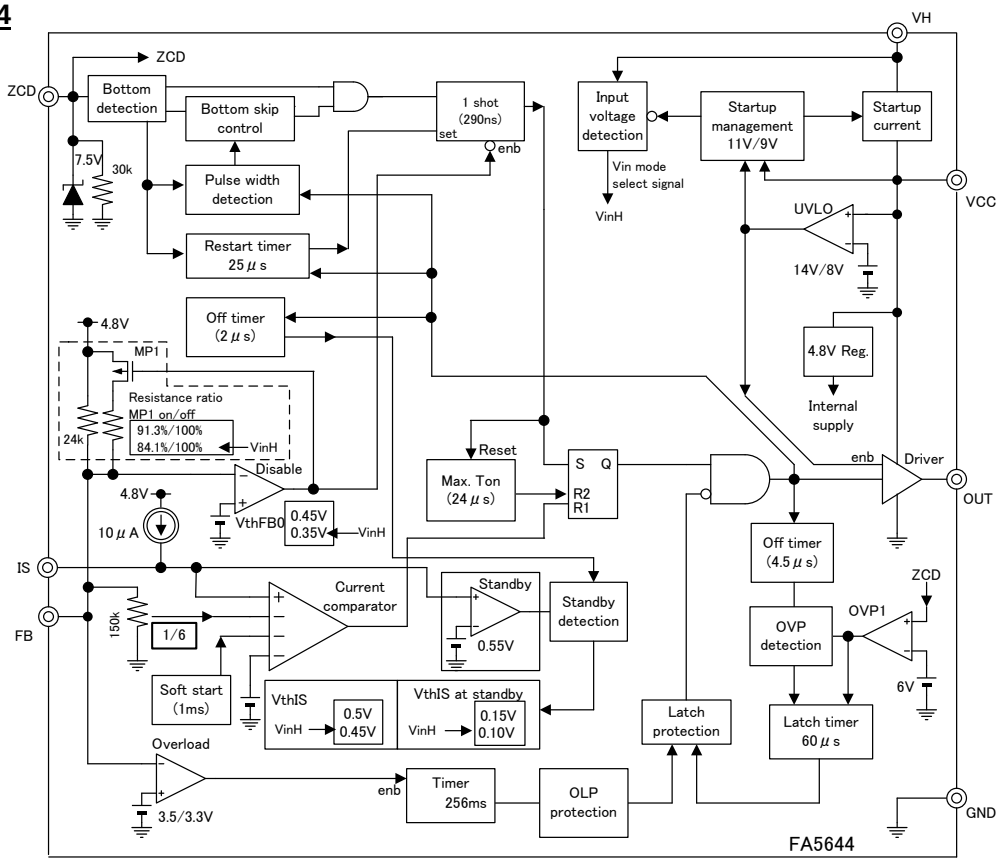

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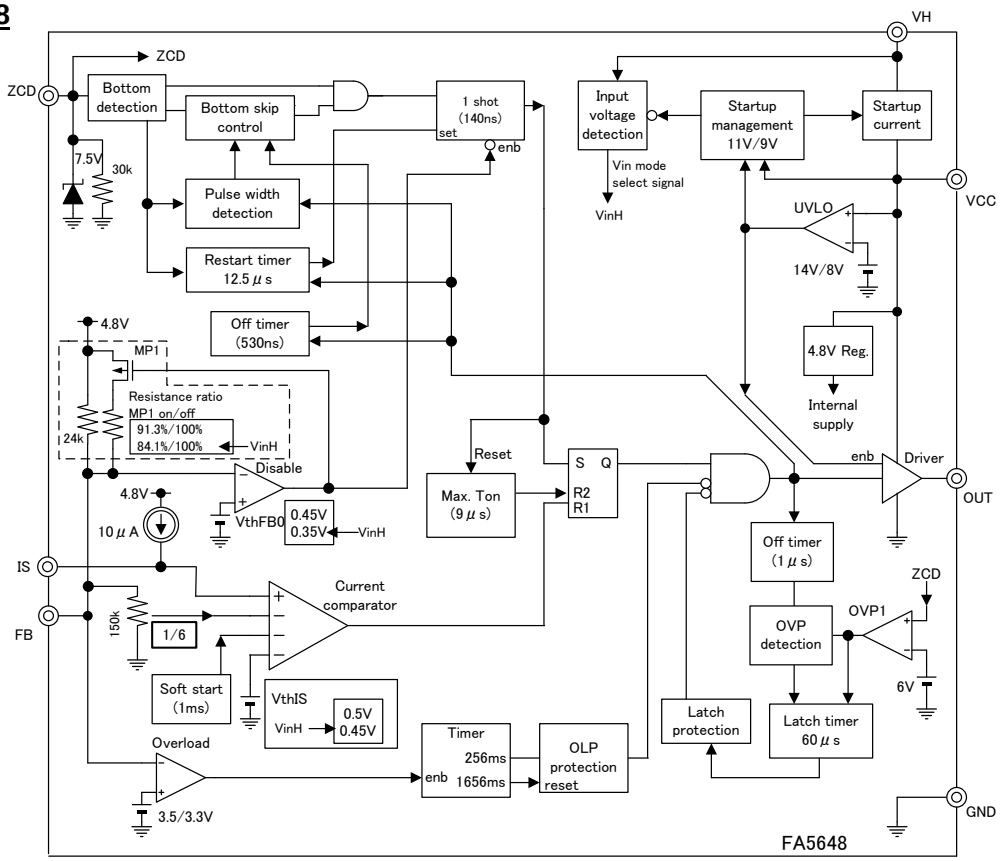


5. Functional description of pins

Pin number	Pin name	Pin function
1	ZCD	Zero current detection, OVP detection
2	FB	Feedback input, OLP detection, Burst operation control
3	IS	Current sense input, Over-current limiter, Standby signal detection
4	GND	Ground
5	OUT	Output
6	VCC	Power supply, UVLO, VH pin current control
7	(N.C.)	（No connection）
8	VH	High voltage input

6. Rating and characteristics

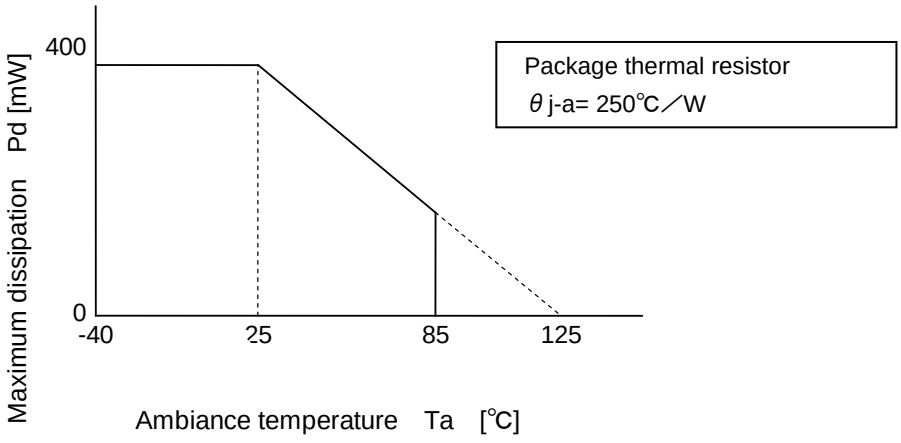
* “+” shows sink and “–“ shows source in current prescription.

(1) Absolute maximum ratings

Item	Symbol	Rating	Unit
Supply voltage	Vcc	28	V
Peak current at OUT pin (Note 1)	IoH	-0.25	A
	IoL	+0.5	A
The voltage at OUT pin	Vout	-0.3 to Vcc+0.3	V
Input voltage at FB and IS pin	Vfb, Vis	-0.3 to 5.0	V
The current at FB and IS pin	Ifb, Iis	-0.3 to +0.3	mA
The current at ZCD pin	IsoZCD	-2.0	mA
	IsiZCD	+3.0	mA
The voltage at ZCD pin	Vzcd	-2 to +8	V
Input voltage at VH pin	VVH	-0.3 to 500	V
Power dissipation（Ta=25℃）	Pd	400	mW
Operating junction temperature	Tj	-40 to +125	℃
Storage temperature	Tstg	-40 to +150	℃

Note 1) Please consider power supply voltage and load current well and use this IC within maximum power dissipation, operating junction temperature and recommended ambient temperature in operation. The IC may cross over maximum power dissipation at normal operating condition by power supply voltage or load current within peak current absolute maximum rating.

* Allowable loss reduction characteristics



(2) Recommended operating conditions

Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc	11	15	26	V
Input voltage at VH pin	Vvh	50	—	450	V
Capacitance at VCC pin	Cvcc	10	47	220	uF
Turn-off resonant period	Trs	—	2	4	us
Ambient temperature in operation	Ta	-40	—	85	℃

(3) DC Electric characteristics (Unless otherwise specified : VCC=15V, VH=141V, ZCD=0V, FB=3V, IS=open, Tj=25℃)

Current sense part (IS pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input bias current	IIS	Vis=0V	-15	-10	-5	uA
Maximum threshold voltage	VthIS1	Vfb=3.2V, Vvh=141V	0.47	0.5	0.53	V
	VthIS2	FA5640/41/43/44/48 Vfb=3.2V, Vvh=324V	0.42	0.45	0.48	V
Voltage gain	AvIS	ΔVfb/ΔVis	5.4	6.0	6.6	V/V
Minimum ON pulse width	Tonmin	FA5640/41/42/44 Vfb=3.2V,Vis=1.5V FA5643 Vfb=3.2V,Vis=0.75V	205	290	375	ns
Minimum ON pulse width	Tonmin	FA5643 Vfb=3.2V,Vis=1.5V	95	140	185	ns
Delay to output	TpdIS	FA5640/41/42/44/48 IS input: 0V to 1.5V (Pulse signal) FA5643 IS input: 0V to 0.75V (Pulse signal)	30	70	150	ns
Latch shutdown threshold voltage	VthISat	FA5643	0.9	0.97	1.1	V

Feedback part (FB pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input threshold voltage of stopping on-pulse	VthFB01	DUTY=0% Vvh=141V	405	450	495	mV
	VthFB02	FA5640/41/43/44/48 DUTY=0% Vvh=324V	315	350	385	mV
FB pin input resistance	Rfb11	Vfb=1V to 2V Vvh=141V	14.2	18.9	23.6	kΩ
	Rfb12	FA5640/41/43/44/48 Vfb=1V to 2V Vvh=324V	13.0	17.4	21.7	kΩ
	Rfb21	Vfb=0V to 0.3V Vvh=141V	15.5	20.7	25.9	kΩ
	Rfb22	FA5640/41/43/44/48 Vfb=0V to 0.3V Vvh=324V	15.5	20.7	25.9	kΩ
FB pin source current	Ifb0	Vfb=0V	-260	-200	-160	uA
FB pin input resistance ratio	⊿Rfb1	⊿Rfb1=Rfb11/Rfb21 Vvh=141V	89.3	91.3	93.3	%
	⊿Rfb2	FA5640/41/43/44/48 ⊿Rfb2=Rfb12/Rfb22 Vvh=324V	82.1	84.1	86.1	%

Zero current detection part (ZCD pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input threshold voltage	Vthzcd1	Vzcd decreasing	40	60	80	mV
	Vthzcd2	Vzcd increasing	100	150	220	mV
Hysteresis	Vhyzcd	Vthzcd2-Vthzcd1	30	90	150	mV
Minimum detectable pulse width	Tzcdmin	ZCD input pulse Vpulse=1V to 0V f=100kHz	300	—	—	ns
Input clamp voltage	Vih	Izcd=+3mA (high state)	6.5	7.5	9.5	V
	Vil	Izcd=-2mA (low state)	-1.0	-0.8	-0.4	V
ZCD pin internal resistance	Rzcd	Vzcd=1V to 5V	22.5	30	37.5	kΩ
ZCD pin propagation delay time	Tzcd	ZCD pulse:1V to 0V, OUT: turn-on	50	150	300	ns
The ON/OFF pulse width of changed number of bottom at turn-on (FA5640/41/42/43/44)	Tb12	Changed 1st bottom to 2nd bottom	8.1	9.0	9.9	us
	Tb21	Changed 2nd bottom to 1st bottom	12.6	14.0	15.4	us
	Tb23	Changed 2nd bottom to 3rd bottom	7.2	8.0	8.8	us
	Tb32	Changed 3rd bottom to 2nd bottom	10.5	11.67	12.84	us
	Tb34	Changed 3rd bottom to 4th bottom	6.3	7.0	7.7	us
	Tb43	Changed 4th bottom to 3rd bottom	9.0	10.0	11.0	us
The ON/OFF pulse width of changed number of bottom at turn-on (FA5648)	Tb12	Changed 1st bottom to 2nd bottom	3.45	3.83	4.21	us
	Tb21	Changed 2nd bottom to 1st bottom	4.95	5.50	6.05	us
	Tb23	Changed 2nd bottom to 3rd bottom	3.15	3.50	3.85	us
	Tb32	Changed 3rd bottom to 2nd bottom	4.35	4.83	5.31	us
	Tb34	Changed 3rd bottom to 4th bottom	2.85	3.17	3.49	us
	Tb43	Changed 4th bottom to 3rd bottom	3.75	4.17	4.59	us
Timeout after last ZCD trigger	Trestart	FA5640/42/43/44 OUT=low, Vzcd=0V	20	25	30	us
		FA5641 OUT=low, Vzcd=0V	6.7	7.6	8.5	us
		FA5648 OUT=low, Vzcd=0V	10	12.5	15	us

Over-voltage protection part (ZCD pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Over-voltage threshold voltage	Vovp	Vzcd is increased, and timer latch function is operated	5.7	6.0	6.3	V
Over-voltage detection timing	Tlat1	FA5640/41/42/43/44 Delay from turn-off	3.5	4.5	5.5	us
		FA5648 Delay from turn-off	0.8	1.0	1.3	us
Delay time to latch-off	Tlat2	Delay from upper the Vovp voltage	40	60	80	us

Overload protection part (FB pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OLP threshold voltage	Volp1	Vfb increasing	3.3	3.5	3.8	V
	Volp2	Vfb decreasing	3.0	3.3	3.6	V
Hysteresis	Hysolp	Volp1-Volp2	0.1	0.2	0.3	V
Fault time duration	Tolp	FA5640/41/42/43 Delay from Vfb>Volp1	140	200	260	ms
		FA5644 Delay from Vfb>Volp1	195	256	320	ms
		FA5648 Delay from Vfb>Volp1	200	256	333	ms
Auto recovery mode latch-off time duration	Toff	FA5640/41/42/43 The OFF time only by internal signal	980	1400	1820	ms

Soft start part

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Soft-start time	Tsoft	at start-up only	0.7	1.0	1.3	ms

Standby-mode function (IS pin) (FA5640,FA5641,FA5642,FA5644)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Stand-by detection threshold voltage at IS pin	VISstb	Read timing is turn-off after Tstb.	0.5	0.55	0.6	V
Stand-by detection timing	Tstb	Delay from turn-off	1.5	2.0	2.5	us
Maximum threshold voltage at stand-by	VthISst1	Vfb=3.2V Vvh=141V	0.12	0.15	0.18	V
	VthISst2	FA5640/41/44 Vfb=3.2V Vvh=324V	0.07	0.10	0.13	V

Other protection part

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum on pulse width	Tonmax	FA5640/41/42/43/44 Vis=0V, Vis=2V Vzcd=0V	20	24	28	us
		FA5648 Vis=0V, Vis=2V Vzcd=0V	8	9	10	us
Minimum switching frequency	Fmin	FA5641/43 Vis=0V,Vfb=3.2V	20.8	25	30.3	kHz

Drive Output part (OUT pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
OUT Low voltage	VOL	IOL=100mA Vcc=15V	0.5	1.0	2.0	V
OUT High voltage	VOH	IOH=-100mA, Vcc=15V	12	13.2	14.5	V
Rise time	tr	Vcc=15V, CL=1nF Tj=25℃	20	40	80	ns
Fall time	tf	Vcc=15V, CL=1nF Tj=25℃	12.5	25	60	ns

High voltage input part (VH pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Current of VH pin	IVHrun	Vvh=400V, Vcc > Vstoff	10	30	60	uA
	IVH1	Vvh=100V, VCC=6.5V	4.0	8.0	10.5	mA
	IVH0	Vvh=100V, VCC=0V	0.49	0.7	1.4	mA
Charge current for VCC pin	Ipre1	Vcc=8V, Vvh=100V	-10	-7.4	-3.7	mA
	Ipre2	Vcc=13V, Vvh=100V At UVLO mode	-9	-5.7	-3	mA
The threshold voltage to change input voltage mode setting at DC input	VHdcH	FA5640/41/43/44/48 Vcc>Vstoff VH pin input voltage is increasing by DC voltage.	200	226	250	V
	VHdcL	FA5640/41/43/44/48 Vcc>Vstoff VH pin input voltage is decreasing by DC voltage.	190	212	235	V
Hysteresis voltage width at DC input only	VHdcHys	FA5640/41/43/44/48 VH: DC voltage input VHdcH-VHdcL	8	14	18	V
The threshold voltage to change input voltage mode setting at AC input (AC RMS conversion voltage)	VHac	FA5640/41/43/44/48 Vcc>Vstoff VH pin input Voltage is half-wave rectified AC waveform.	141	160	177	Vrms
Delay time of changing input voltage mode setting	TpdVH	FA5640/41/43/44/48 Vcc>Vstoff (VCC charge off)	11	30	70	ms

Low voltage malfunction protection circuit (UVLO) part (VCC pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start-up threshold voltage	VCCon	FA5640/41/43/44/48 Vcc Increasing	12.5	14	15.5	V
		FA5642 Vcc Increasing	9	10	11	V
Shutdown threshold voltage	VCCoff	Vcc decreasing	7	8	9	V
Hysteresis (UVLO)	Vhys1	FA5640/41/43/44/48 VCCon-VCCoff	5	6	7	V
Istart-up off voltage		FA5642 VCCon-VCCoff	1.5	2	2.5	V
Istart-up restart voltage	Vstoff	Vcc Increasing	9.5	11	12.5	V
Hysteresis width at Istart-up	Vstrst	Vcc decreasing	8	9	10	V

Current consumption (VCC pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating-state supply current	ICCop1	FA5640/41/42/44/48 Vfb=2V, IS=open Vzcd=0V OUT= no load FA5643 Vfb=2V, IS=0.75 Vzcd=0V OUT= no load	0.7	0.85	1.5	mA
	ICCop2	FA5640/41/42/44/48 Duty cycle=0%, Vfb=0V, IS=open Vzcd=0V FA5643 Duty cycle=0%, Vfb=0V, IS=0.75 Vzcd=0V	0.6	0.8	1.1	mA
Latch mode supply current	ICClat	FB=open Vcc=11V At latch-mode	100	200	350	uA

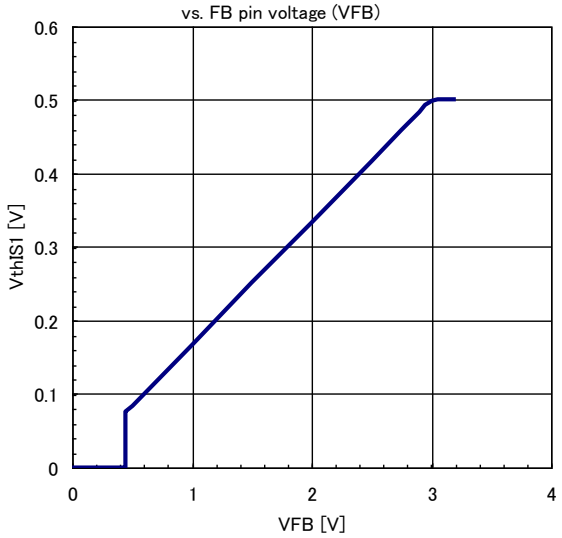
*1 : Regarding to these items, guaranteed by design.

The column showing '-' has no specified value.

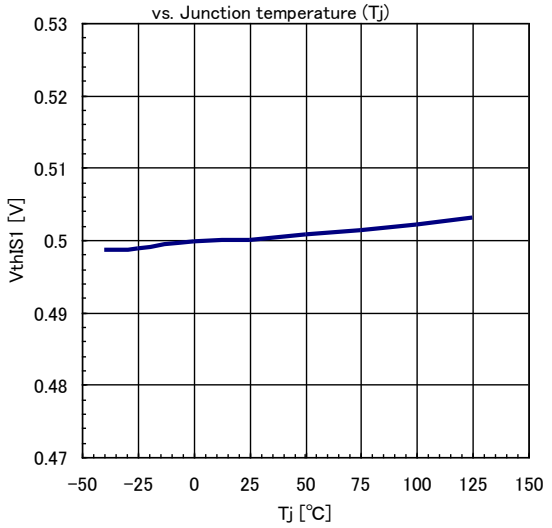
7. Characteristic curve

- Unless otherwise specified : Tj=25℃, VCC=15V
- “+” shows sink and “–“ shows source in current prescription.
- Data listed here shows the typical characteristics of an IC and does not guarantee the characteristics.

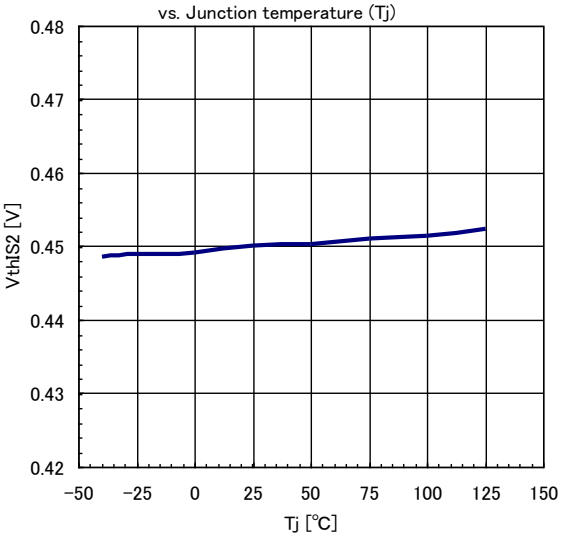
IS pin maximum threshold voltage (VthIS1)
vs. FB pin voltage (VFB)



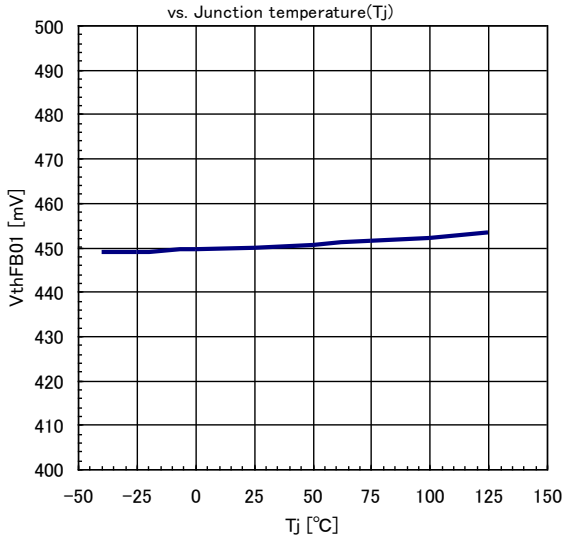
IS pin maximum threshold voltage (VthIS1)
vs. Junction temperature (Tj)



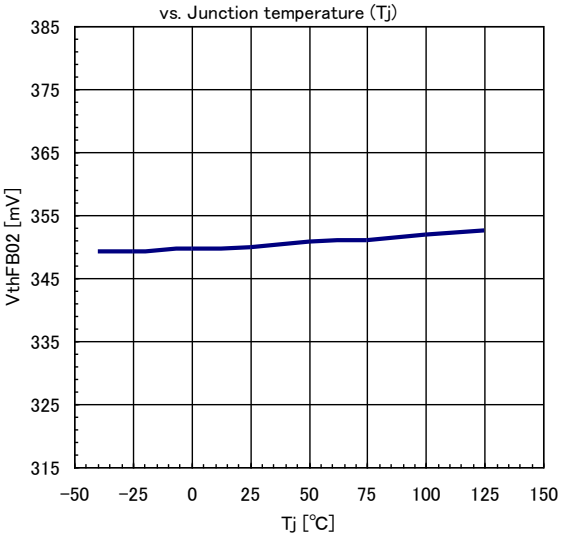
IS pin maximum threshold voltage (VthIS2)
vs. Junction temperature (Tj)



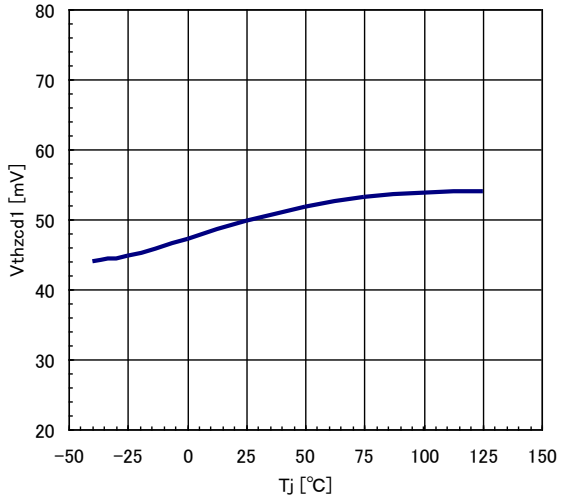
FB pin input threshold voltage switching off (VthFB01)
vs. Junction temperature(Tj)



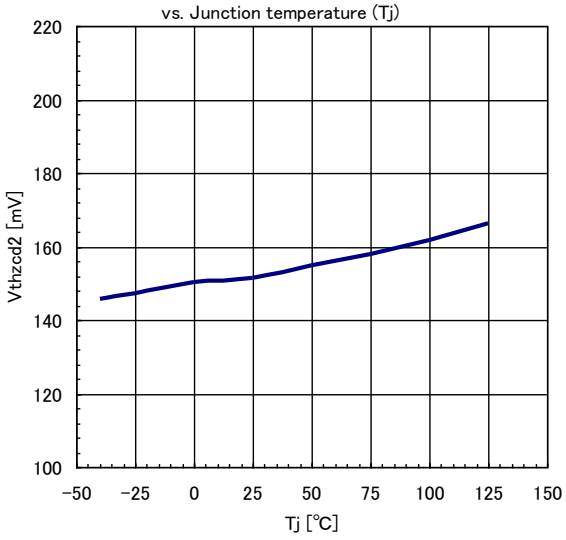
FB pin input threshold voltage switching off (VthFB02)
vs. Junction temperature (Tj)



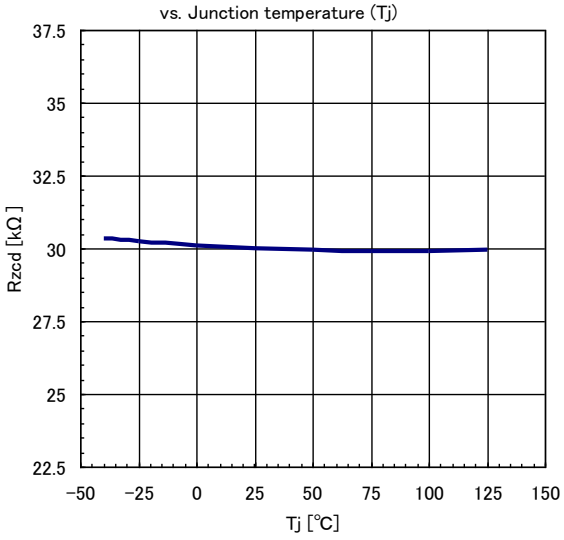
ZCD pin input threshold voltage (Vthzcd1)
vs. Junction temperature (Tj)



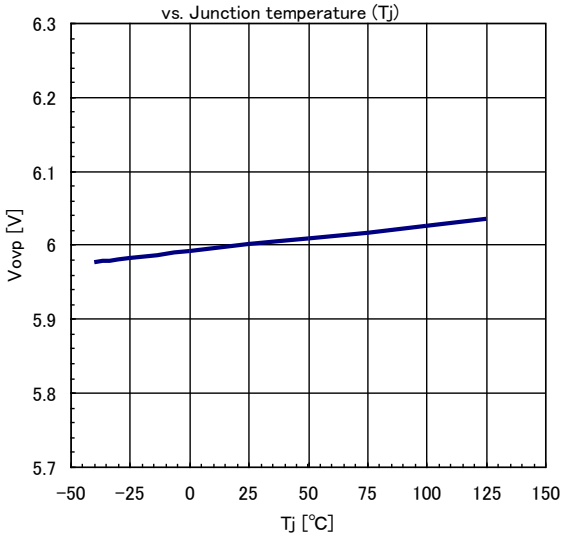
ZCD pin input threshold voltage (Vthzcd2)
vs. Junction temperature (Tj)



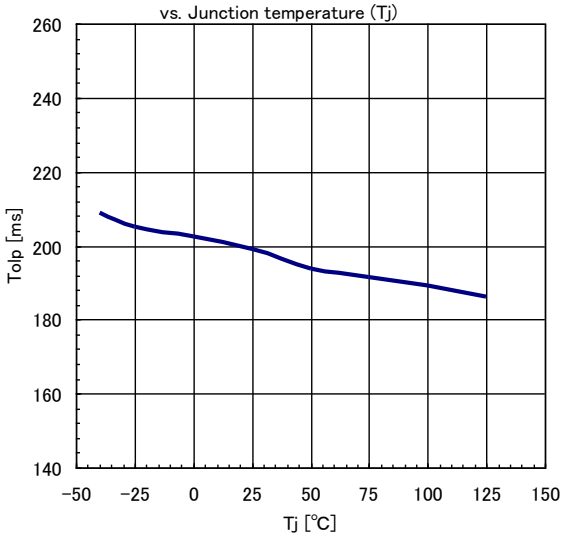
ZCD pin internal resistance (Rzcd)
vs. Junction temperature (Tj)



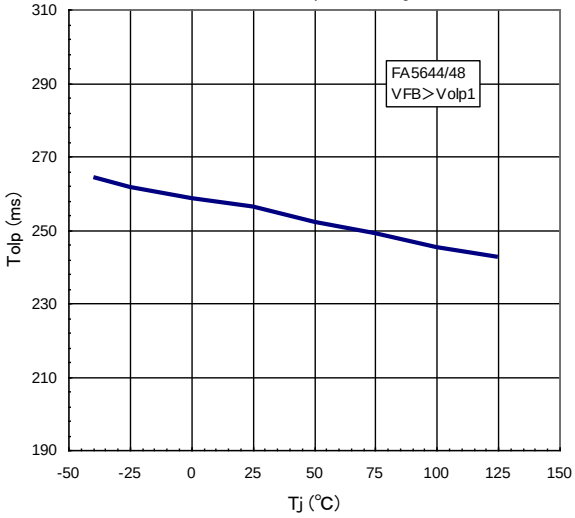
ZCD pin OVP threshold voltage (Vovp)
vs. Junction temperature (Tj)



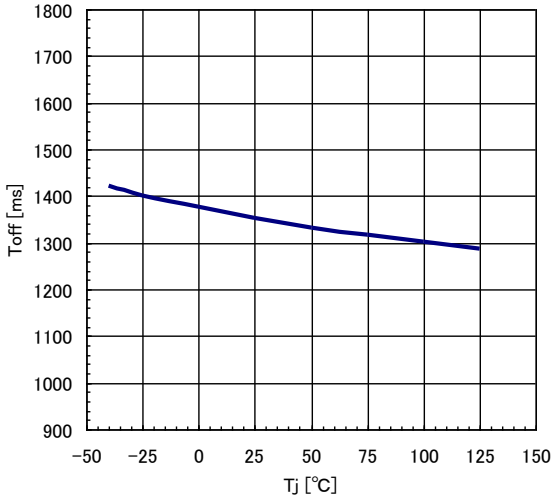
Delay time to OLP (Tolp)
vs. Junction temperature (Tj)



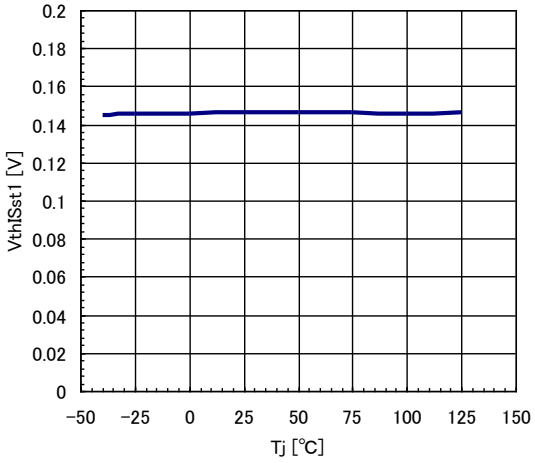
Delay time to OLP (Tolp)
vs. Junction temperature (Tj)



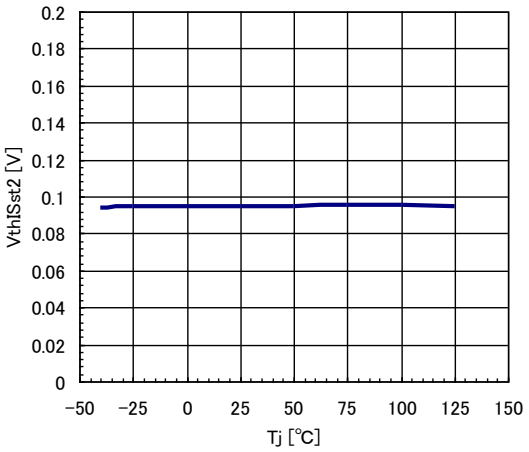
OLP off time (Toff)
vs. Junction temperature (Tj)



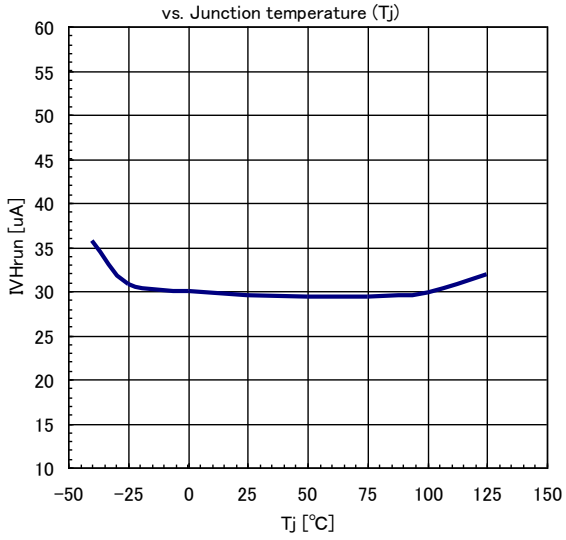
IS pin maximum threshold voltage at standby
(VthISst1)
vs. Junction temperature (Tj)



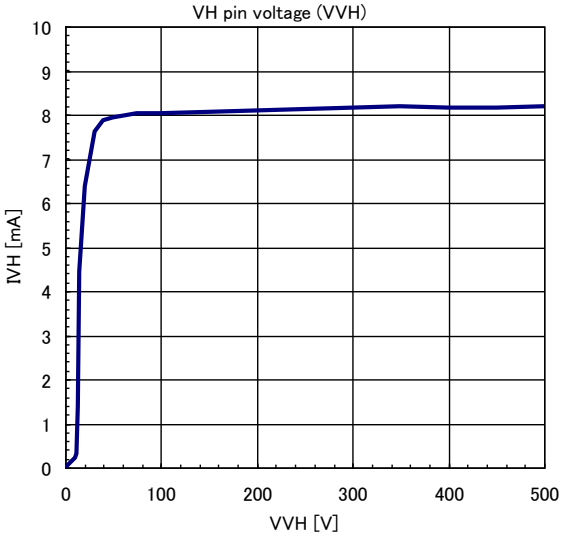
IS pin maximum threshold voltage at standby
(VthISst2)
vs. Junction temperature (Tj)



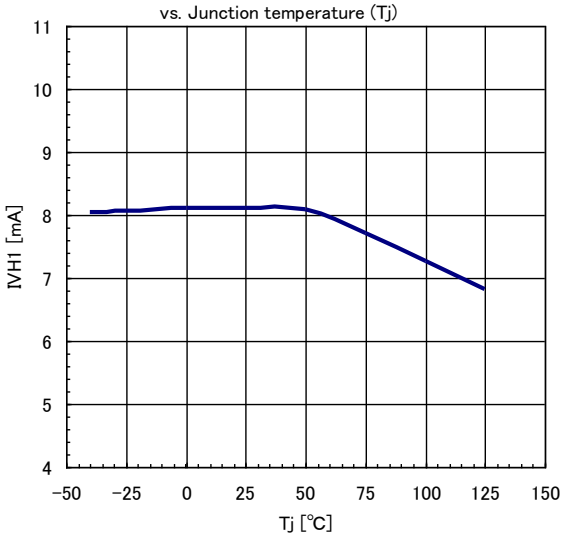
Input current of VH pin (IVHrun)
vs. Junction temperature (Tj)



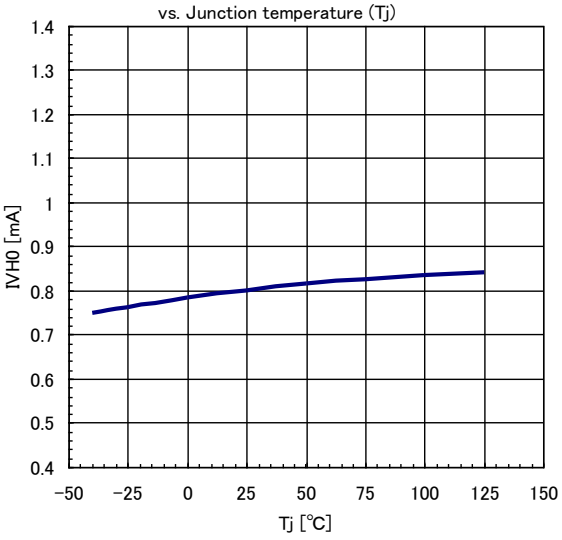
Input current of VH pin (IVH)
VH pin voltage (VVH)



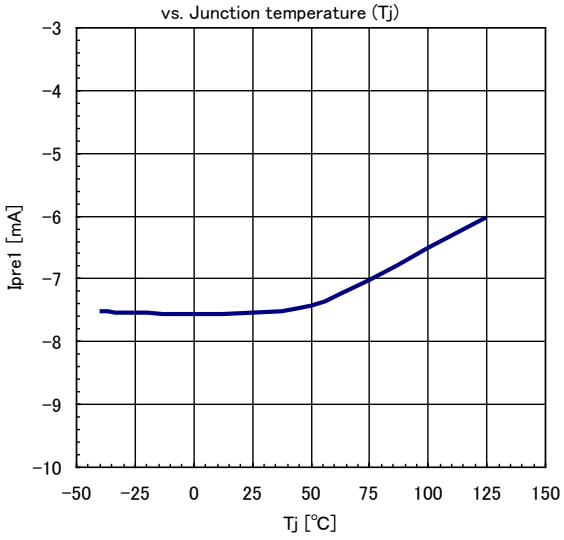
Input current of VH pin (IVH1)
vs. Junction temperature (Tj)



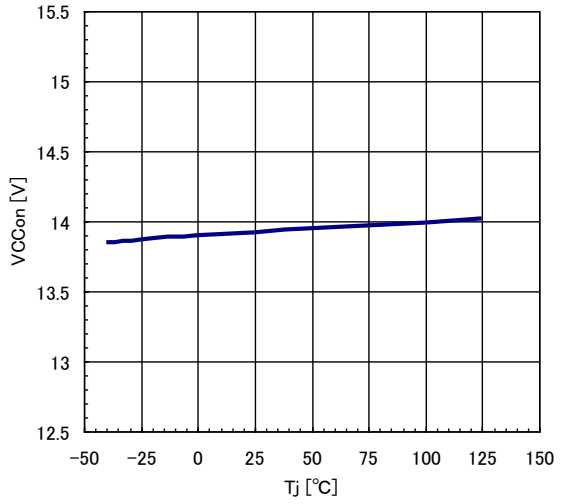
Input current of VH pin (IVH0)
vs. Junction temperature (Tj)



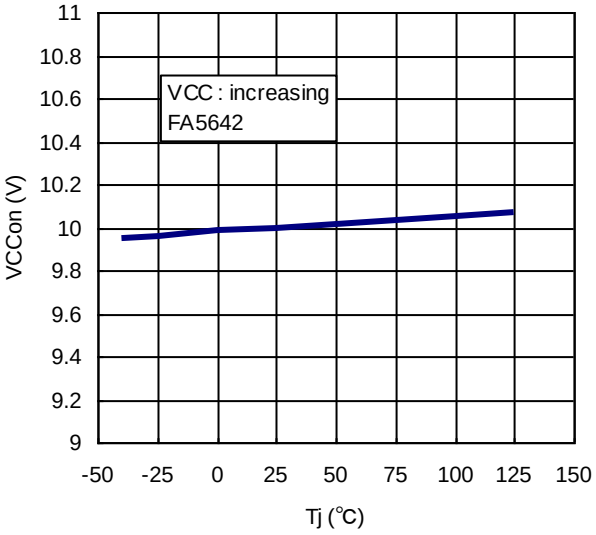
Charge current for VCC pin (Ipre1)
vs. Junction temperature (Tj)



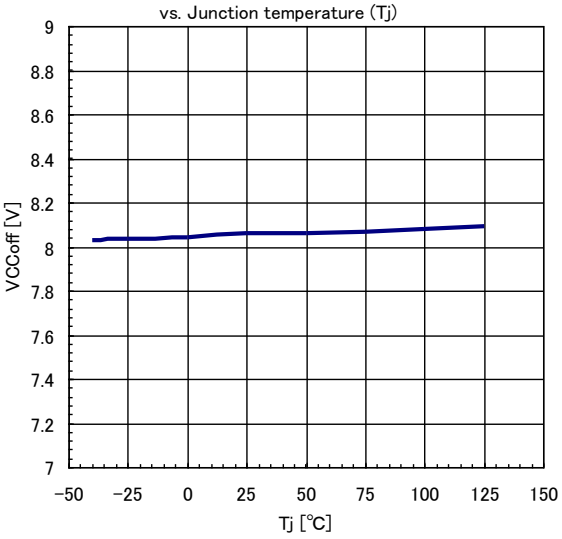
Startup threshold voltage (VCCon)
vs. Junction temperature (Tj)



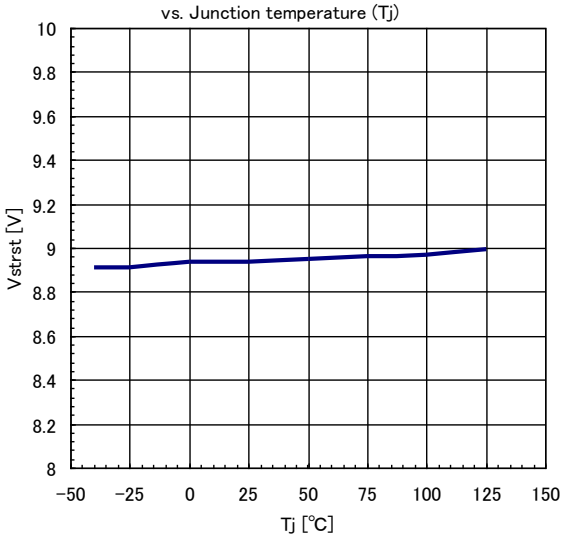
UVLO ON threshold voltage (VCCon)
vs. Junction temperature (Tj)



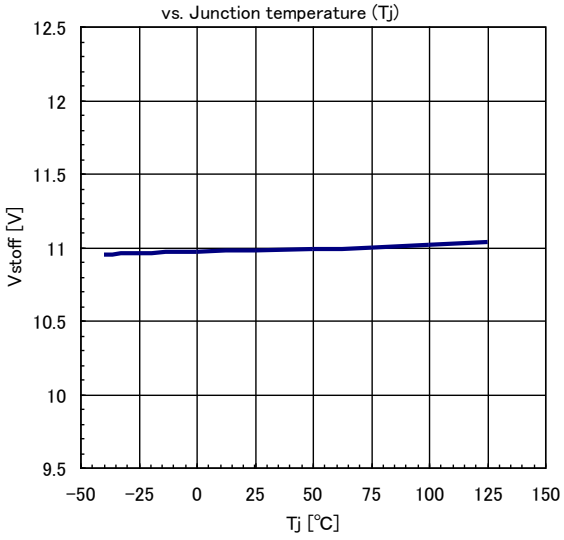
Shutdown threshold voltage (VCCoff)
vs. Junction temperature (Tj)



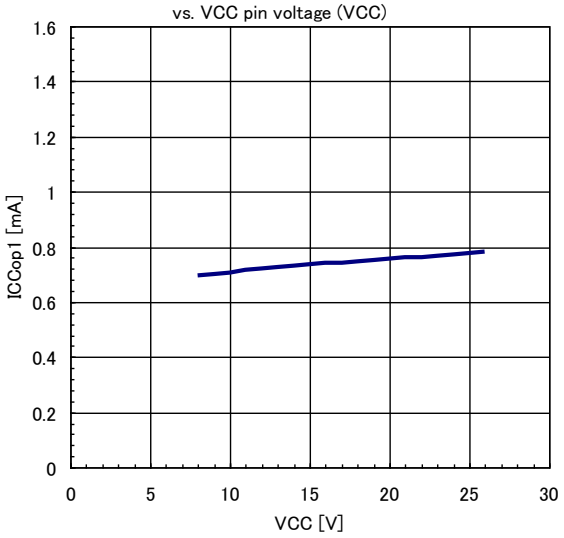
Startup device ON voltage (Vstrst)
vs. Junction temperature (Tj)



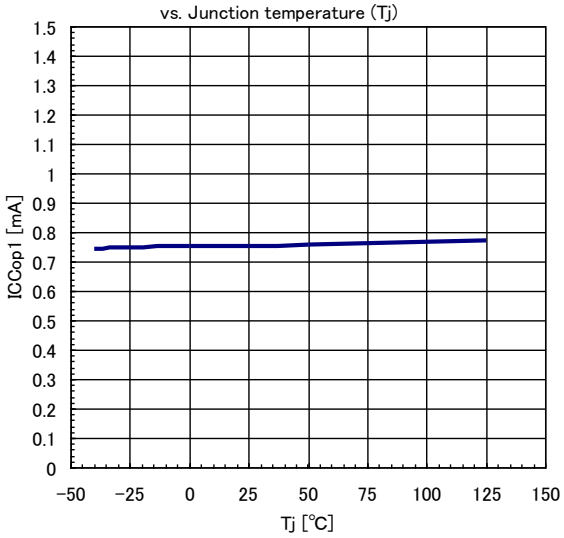
Startup device OFF voltage (Vstoff)
vs. Junction temperature (Tj)



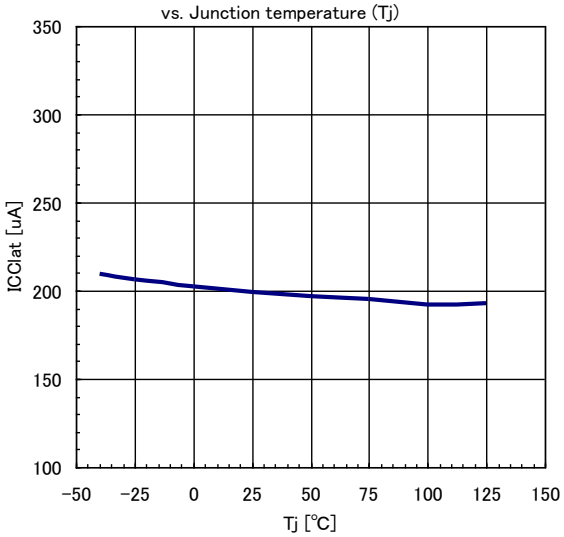
Operating-state supply current (ICCop1)
vs. VCC pin voltage (VCC)



Operating-state supply current (ICCop1)
vs. Junction temperature (Tj)



Latch mode supply current (ICClat)
vs. Junction temperature (Tj)



8. Basic operation (The values in the following description are typical values unless otherwise specified.)

The basic operation of the power supply using IC is not switching operation with fixed frequency using an oscillator but switching with self-excited oscillation. This is shown in Fig.1 Schematic circuit diagram and Fig.2 Waveform in the basic operation.

t1 to t2

Q1 turns ON and then Q1 drain current Id (current of primary windings of T1) begins to rise from zero. Q1 current is converted into the voltage by Rs and is input into IS pin.

t2

When the current of Q1 get to the reference voltage of the current comparator that is fixed by the voltage of FB pin, a reset signal is input into RS flip-flop and Q1 turns OFF.

t2 to t3

When Q1 turns OFF, then the windings voltage of the transformer turns over and the current IF is provided from the transformer into the secondary side through D1.

t3 to t4

When the current from the transformer into the secondary side stops and the current of D1 gets to zero, the voltage of Q1 turns down rapidly due to the resonance of the transformer inductance and the capacitor Cd. At the same time the transformer auxiliary windings voltage Vsub also drops rapidly.

ZCD pin receives this auxiliary windings voltage but then it has a little delay time because of CR circuit composed with RZCD and CZCD on the way.

t4

If ZCD pin voltage turns down lower than the threshold voltage 50mV of Bottom detection, a set signal is input into R-S flip-flop and Q1 turns ON again. If the delay time of CR circuit placed between the auxiliary windings and ZCD pin is adjusted properly, Q1 voltage can be turned on at the bottom. This operation makes the switching loss of TURN ON to the minimum.

(Return to t1)

Subsequently repeat from t1 to t4 and continue switching.

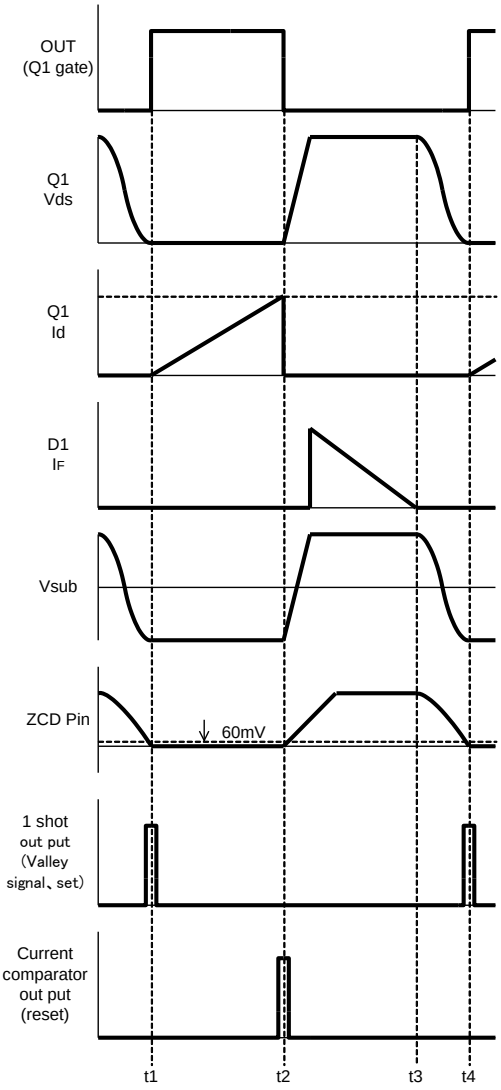


Fig.2 Waveform in basic operation

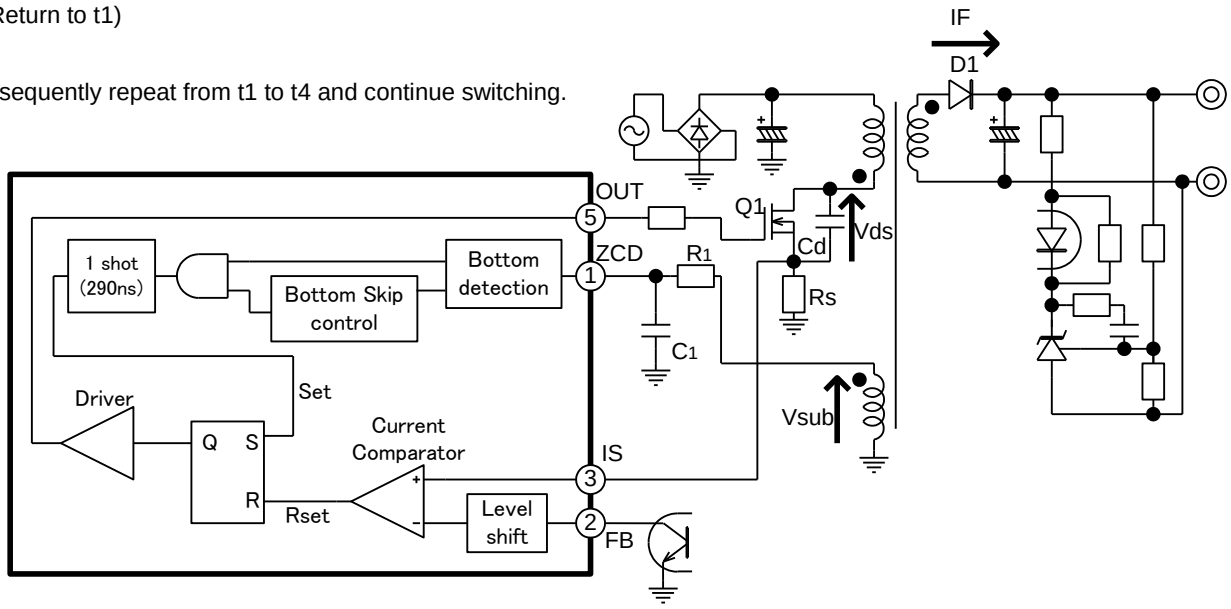


Fig.1 Schematic circuit diagram in basic operation

9. Description of the function (The values in the following description are typical values unless otherwise specified.)

(1) Steady-state operation, bottom-skip operation, and burst operation

• Steady-state operation, bottom-skip operation (FA5640/41/42/43/44/48 *FA5648:See spec. of P10)

The ON/OFF cycle, which is from turn-on of the driver signal to the end of fly-back voltage, is detected, and bottom-skip operations are performed at the time detected. Since the relation between the ON/OFF width and the number of times of bottom skip operations is exhibited in the hysteresis as shown in Fig. 4, waveform fluctuations can be prevented and transformer audible noise can be decreased. Fig. 5 shows the change image of the switching frequency to the output electric power. Fig. 6 shows the change image of the ON/OFF width.

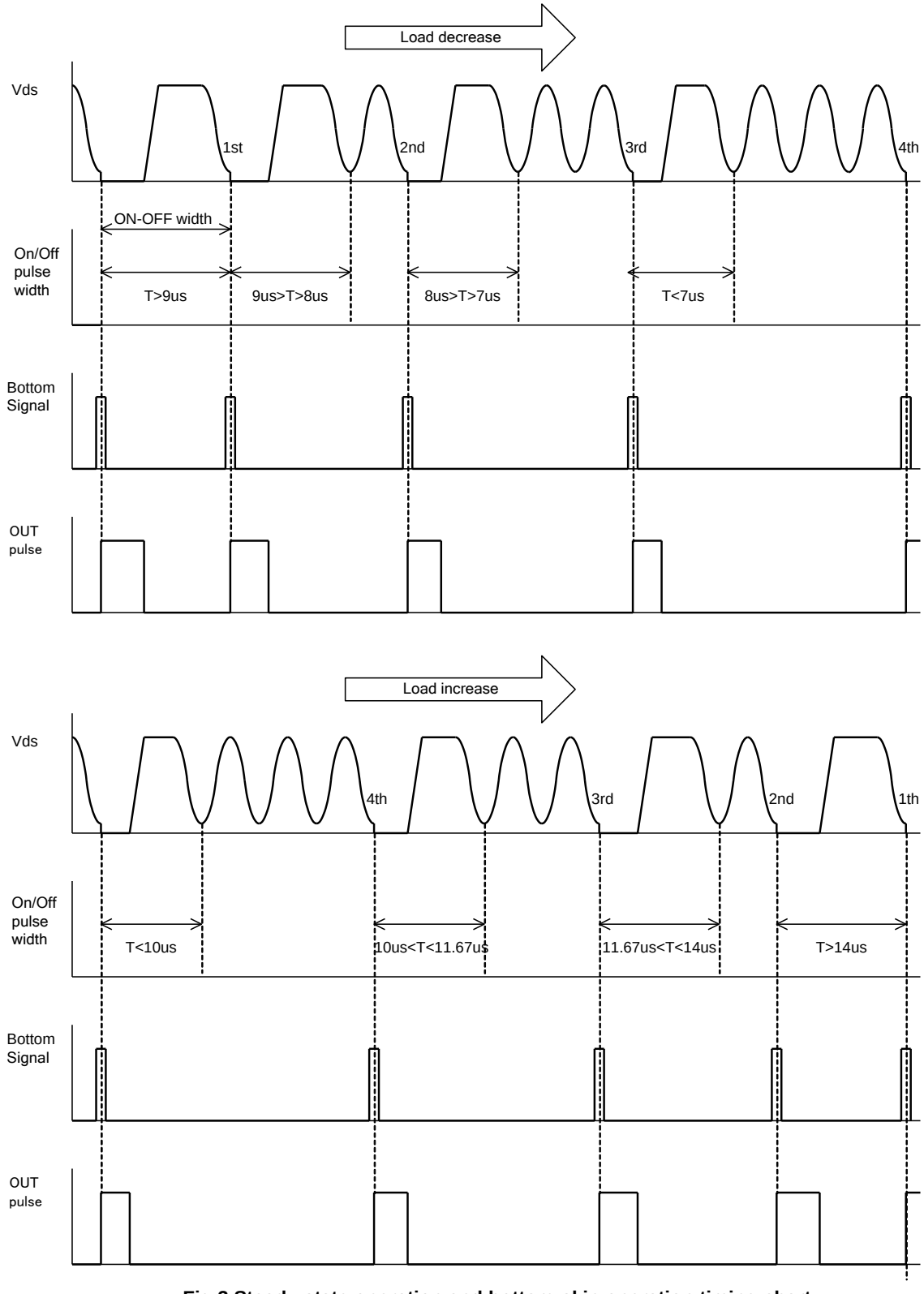


Fig.3 Steady-state operation and bottom-skip operation timing chart

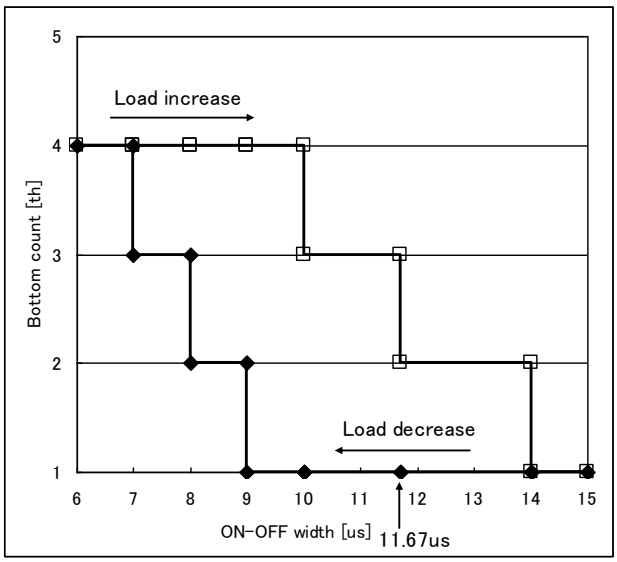


Fig.4 ON/OFF width at transfer to bottom-skip operation

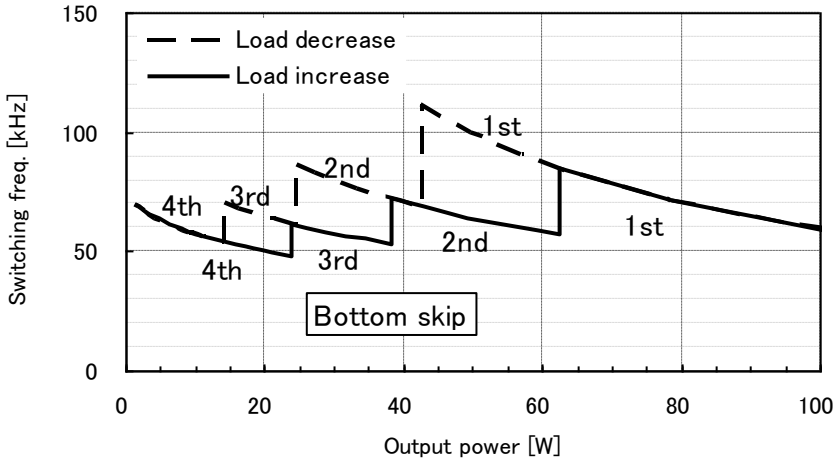


Fig.5 Change image of switching frequency

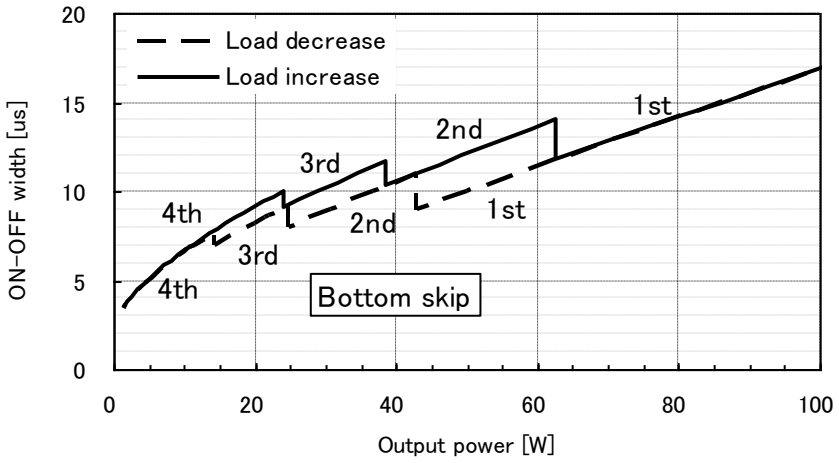


Fig.6 Change image of ON/OFF width

• Burst operation

When the FB pin voltage decreases to lower than the pulse shutdown threshold voltage, switching is stopped. On the contrary, if the FB voltage increases to higher than the pulse shutdown threshold voltage, switching is resumed. Overshoot and undershoot of the FB pin voltage occur over and under the pulse shutdown threshold voltage for mode switching. Continuous pulses are issued during this overshoot period, and long-cycle burst frequency is obtained during the undershoot period. The pulse shutdown threshold voltage is switched to 0.45 V when input voltage is low, whereas it is switched to 0.35 V when input voltage is high, as input voltage compensation.

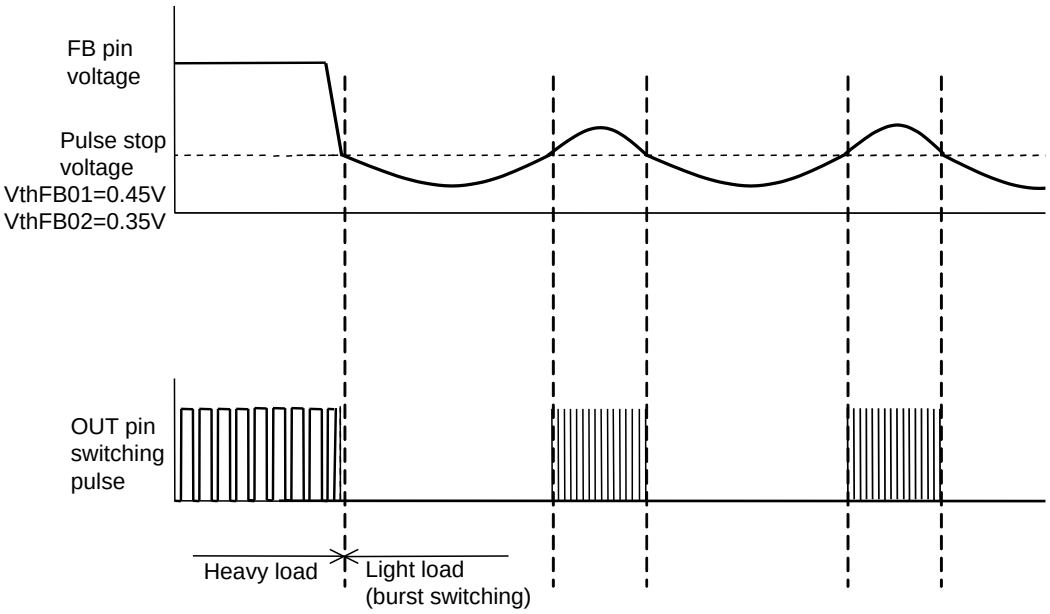


Fig.7 Burst operation at light load

(2) Startup circuit and auxiliary winding voltage

When power is turned on, the current supplied from the startup circuit to the VCC pin through the VH pin charges the capacitor connected to the VCC pin to increase voltage. If the VCC pin voltage exceeds ON threshold voltage 14 V or 10 V, the internal operation power is turned on, and the IC is start operating. At this time, if the voltage supplied from the auxiliary winding is higher than 9 V, the startup circuit is operated at the time of startup only, and after the startup, auxiliary winding voltage is used as power supply. Meanwhile, if the auxiliary winding voltage is lower than 9V, the IC maintains operation within the VCC range between 9V and 11V by ON/OFF of startup circuit.

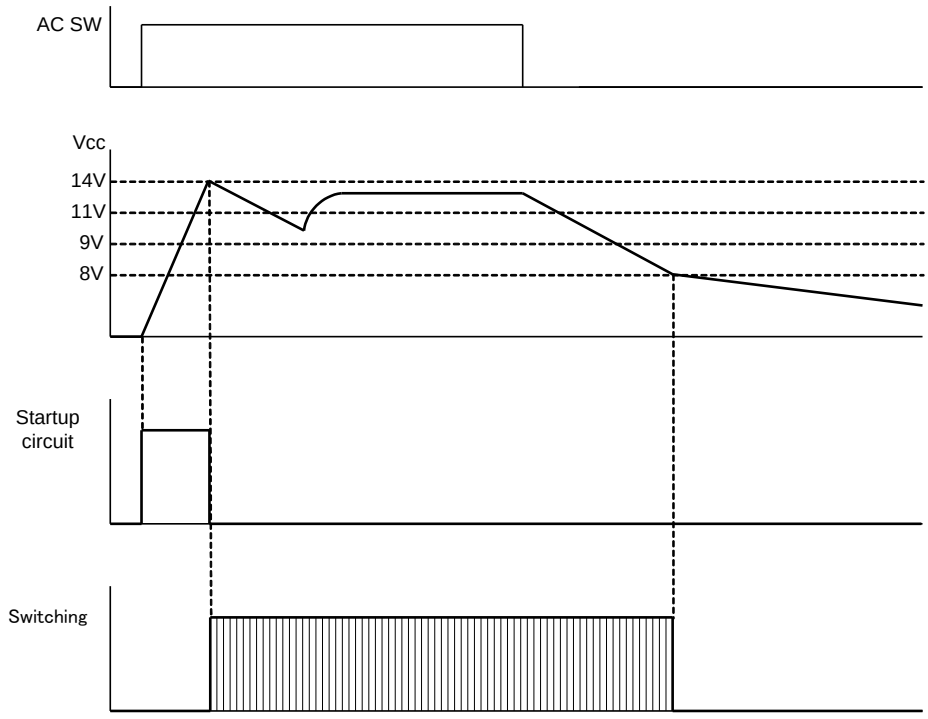


Fig.8 Startup and shutdown (When auxiliary winding voltage is higher than 9V)

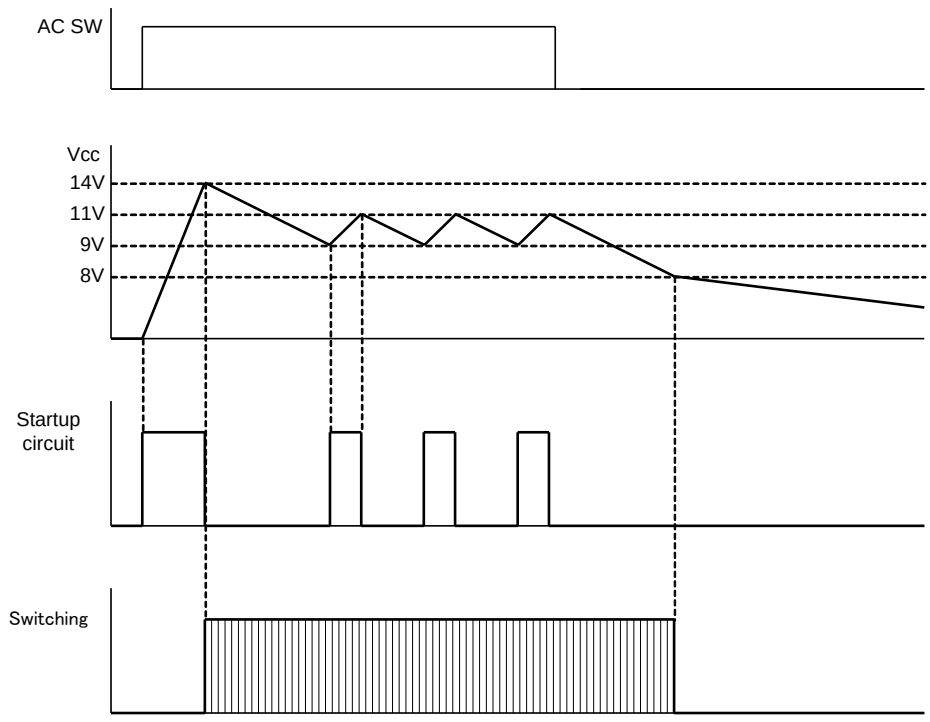


Fig.9 Startup and shutdown (When auxiliary winding voltage is lower than 9V)

(3) Operation under overload

■Auto recovery type (FA5640/41/42/43/48 *FA5648: OLP Fault time duration=256ms)

Using the built-in timer, the duration of overload status of 200 ms or longer is detected, and switching is stopped forcibly. If the switching is stopped, supply of current from the auxiliary winding is eliminated, and the VCC pin voltage reduces to 9 V or lower, the startup circuit is operated, and the VCC is maintained within the range from 9 V to 11 V. If overload status continues for 200 ms or longer, the switching is stopped, and then after the elapse of 1400 ms, the switching is resumed. At that time, if the overload status persists, start and stop switching are repeated. If the load returns to normal, normal operation is resumed.

At the time of startup, it is necessary to increase the output voltage to the setting within the timer setting of 200 ms. Since the operation is performed automatically using the built-in timer, even if external power is input directly to the VCC pin, operation is reset automatically.

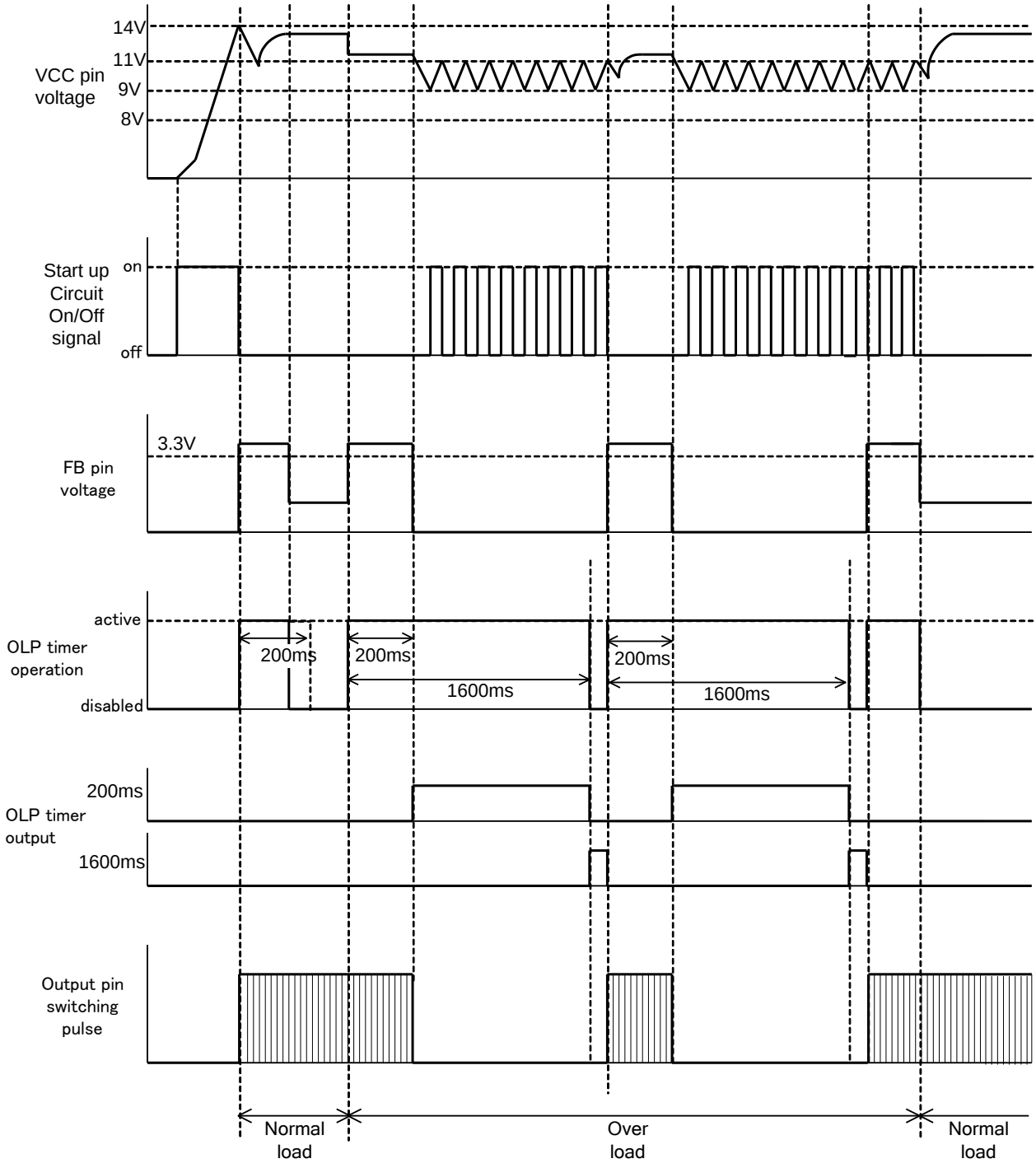


Fig.10 Operation under overload (Auto recovery type)

■Timer latch type (FA5644)

Using the built-in timer, the duration of overload status of 256 ms or longer is detected, switching is stopped, and latch mode is entered, with this state maintained. In a state in which switching is stopped due to overload latch, VCC is supplied from the startup circuit while operation is suspended. To reset the overload latch, it is necessary to interrupt the input voltage to stop the supply of VCC from the startup circuit, thus decreasing the OFF threshold voltage to 8.0 V or lower.
At the time of startup, it is necessary to increase the output voltage to the setting within the timer setting of 256 ms.

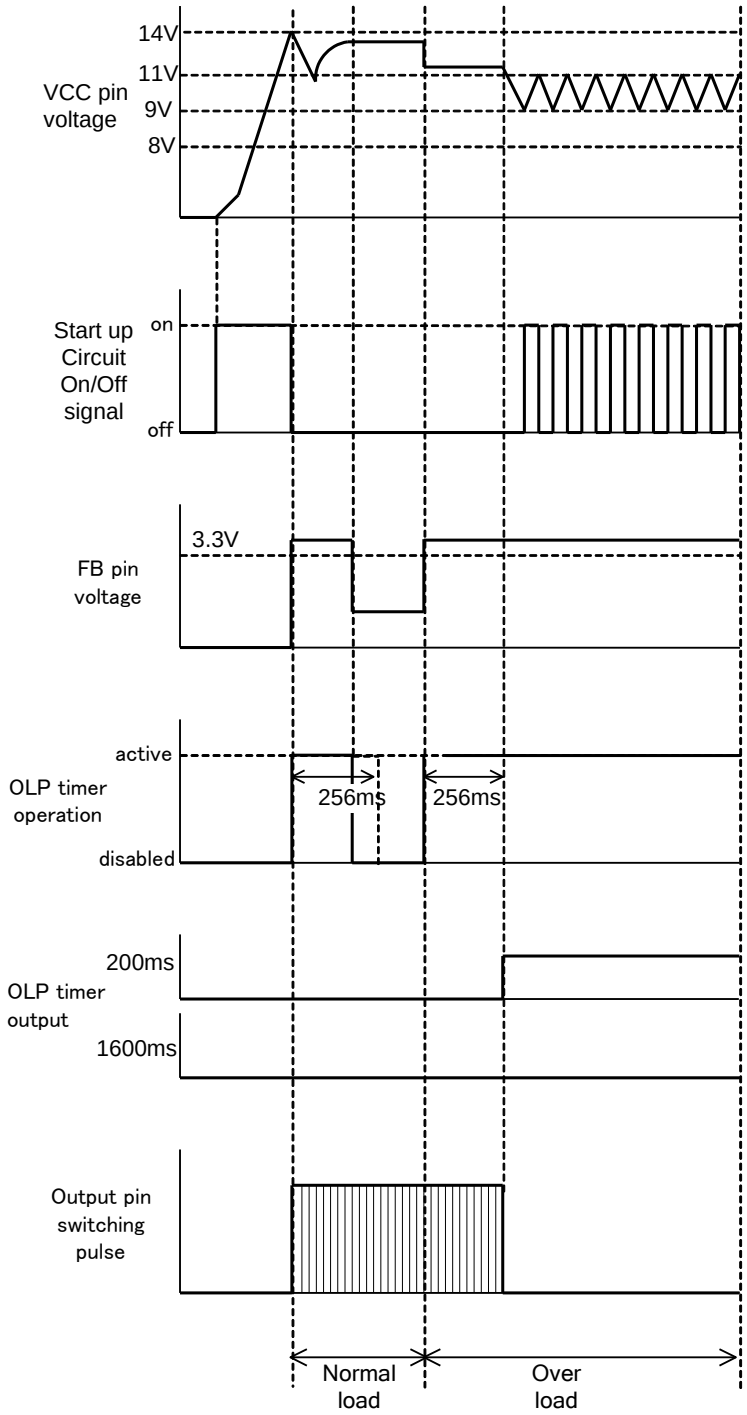


Fig.11 Operation under overload (Timer latch type)

(4) Overvoltage protection function on the secondary side

In case of overvoltage of output, the voltage of the auxiliary winding also rises. The ZCD pin has the function of cycle-by-cycle detecting the voltage of the auxiliary winding of transformer. If the state in which the ZCD pin voltage is 6.0 V or higher continues for 60 μs or longer, switching is stopped and the operation is latched-off. This state is maintained until the input voltage is interrupted, and the VCC decreases to the OFF threshold voltage of the UVLO.

For example if switching is made at 40 kHz, 60 μs × 40 kHz = 2.4: detection of twice or more is required.

(5) External latch-off function

By pulling up the ZCD pin to 6.0 V or higher for 60 μs or longer, the IC is latched-off. This state is maintained until the input voltage is interrupted and VCC decreases to the OFF threshold voltage of the UVLO.

(6) Compensating each threshold level by high-line voltage detection (Except FA5642)

By detecting the peak voltage of the VH pin, each threshold level is switched to compensate for high/low line voltage. The threshold level to be switched by high-line voltage include the pulse shutdown FB voltage, which is related to the pulse mode switching load, and the maximum input threshold voltage, which is the overcurrent limit level of the IS pin.

(7) Minimum switching frequency limitation and maximum ON width limitation

The maximum ON pulse width is limited to 24 μs(FA5648:9μs) to reduce the audible noise of the transformer when it is started and stopped. In addition, FA5641 is integrated in minimum switching frequency that is limited at 25 kHz to reduce audible noise more. See 10. (9) “Other advice on designing” for details.

(8) Switching of overload protection levels due to external signal detection (Standby-mode function) (Except FA5643/48)

By pulling up the voltage of IS pin to higher than the IS pin standby detection voltage during the OFF period of the MOSFET using external signals, overload protection levels can be switched. More specifically, by switching the maximum input threshold voltage, which is the overcurrent limit level of the IS pin, the power can be limited to approximately 1/7 of the overload protection level of normal operation.

This function is useful for limiting the power in standby mode, for example.

(9) Restart operation

If the MOSFET cannot be turned on based on bottom detection of the ZCD pin at the time of startup, restart operation is performed using a timer to forcibly turn on the MOSFET. If the condition in which the OUT is Low (MOSFET is OFF) and the voltage of the ZCD pin is below to input threshold voltage (Vthzcd2) 150 mV or lower, the timer starts counting and the MOSFET is turned ON when the timeout from the last ZCD trigger.

(10) IS pin timer latch function (FA5643)

This IC has function in it that carries out latch shutdown instantly when the voltage higher than 0.97V is impressed to IS pin to protect a transformer short circuit. This state is maintained until the input voltage is interrupted and VCC decreases to the OFF threshold voltage of the UVLO.

10. How to use each pin and advice for designing (The values that appear in the following description are typical values, unless otherwise specified.)

(1) Pin No. 1 (ZCD pin)

Function

(i) Detects the timing that MOSFET is turned on.

(ii)Performs latch-off protection by external signals.

(iii)Performs latch-off protection in case overvoltage on the secondary side.

How to use

(i) Turn on timing detection

• Connection method

Connect the auxiliary winding of the transformer via the CR circuits, R1 and C1 (Fig. 12).

Be careful the polarity of the auxiliary winding.

• Operation

If the voltage of the ZCD pin decreases to 60 mV or lower, the MOSFET is turned on. The auxiliary winding voltage fluctuates significantly in both positive and negative voltage at the time of switching. To protect the IC from this voltage fluctuation, a clamp circuit is integrated. If the auxiliary winding voltage is positive, current is fed as shown in Fig. 13, and if it is negative, current is fed as shown in Fig. 14, to clamp the voltage of the ZCD pin.

In turning ON based on bottom detection of the ZCD pin is not possible at the time of startup, for example, restart operation is performed using timer to forcibly turn on the MOSFET. If the OUT is Low (MOSFET is OFF) and the voltage of the ZCD pin is below to input threshold voltage (Vthzcd2) 150 mV or lower, the timer starts counting, and if the time out time from the last trigger 25 μs (FA5641:7.6 μs,FA5648:12.5 μs), the MOSFET is turned on.

(ii) Latch-off protection by external signals

• Connection method

Pull up the ZCD pin by external signals.

Figure 15 is a typical connection showing the overvoltage on the primary side. (Constants are examples. Check the operation with the actual power supply unit.)

• Operation

If the voltage of the ZCD pin exceeds 6.0 V, and this state continues for 60 μs or longer, latch-off operation is performed to stop output switching.

Once the latch-off operation is started, the VCC voltage is maintained by the startup circuit to continue the latch-off operation.

Decrease the VCC to the OFF threshold voltage or lower to reset the latch operation.

(iii) Latch-off protection at overvoltage on the secondary side

• Connection method

The same as turn on timing in (i)

• Operation

If the output voltage (Vo) on the secondary side enters overvoltage state, the auxiliary winding voltage and ZCD pin voltage also increase. This IC detects ZCD pin voltage elapsed time of 4.5 μs(FA5648:1.0μs) after MOSFET is turned off, and when the ZCD pin voltage exceed 6.0V and this states continues for 60 μs or longer, latch-off operation is performed to stop switching (Fig. 16).

Once the latch operation is started, the VCC voltage is maintained by the startup circuit to continue the latch operation. Decrease the VCC to the OFF threshold voltage of the UVLO or lower to reset the latch operation.

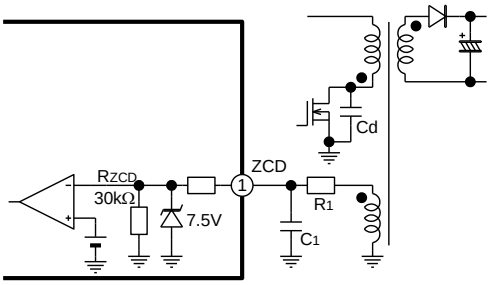


Fig.12 ZCD pin circuit

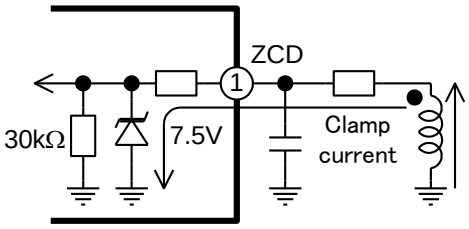


Fig.13 Clamp circuit (When auxiliary winding is in positive voltage.)

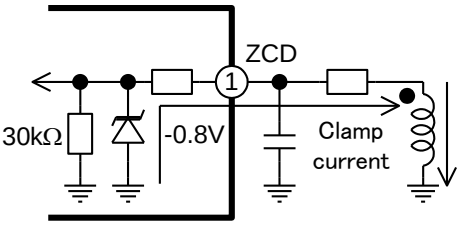


Fig.14 Clamp circuit (When auxiliary winding is in negative voltage.)

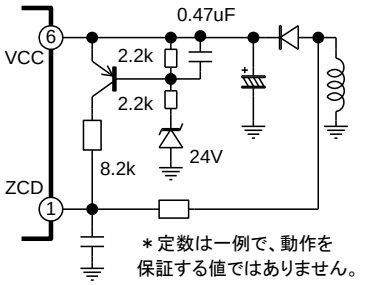


Fig.15 Primary side overvoltage protection circuit

Advice for designing

Immediately before the MOSFET is turned on, the MOSFET drain-source voltage is resonated due to the transformer inductance and the resonance capacitor Cd. Adjust C1 to allow the MOSFET to be turned on at the valley of this resonance (See Figs. 17 and 18).

Since overvoltage threshold voltage is 5.7 V (min.), select resistance R1 not to allow the ZCD pin voltage to exceed 5.7 V, or allow the ZCD pin current to exceed the absolute maximum rating, in normal operation, ensuring that the following calculation formulae are satisfied.

$$V_{ZCD}=V_{thOVP}\times VN_s / V_{OVP}$$

where,

V_{ZCD}: ZCD pin voltage at normal operation

V_{thOVP}: ZCD pin overvoltage threshold level (6 V)

VN_s: Line voltage secondary winding of transformer at normal operation (Vo + VF)

V_{OVP}: Output voltage to be subjected to overvoltage latch-off

$$VN_{sub}=VN_s\times N_{sub} / N_s$$

where,

VN_{sub}: Line voltage of auxiliary winding of transformer

N_{sub}: Number of turns of auxiliary windings of transformer

N_S: Number of turns of secondary windings of transformer

Using the formula

$$V_{ZCD}=VN_{sub}\times R_{ZCD} / (R_1+R_{ZCD}),$$

R1 is found to be

$$R_1=VN_{sub}\times R_{ZCD} / V_{ZCD}-R_{ZCD}$$

where,

R_{ZCD}: Internal resistance of ZCD pin (30 kΩ)

If the capacitance of capacitor C1 is to be increased to prevent malfunction due to surge, for example, it may be necessary to decrease the resistance R1 for bottom detection of the auxiliary winding. If the overvoltage detection level decreases as a result, add resistance R2 for adjustment.

In this case, the following formula applies:

$$R_1=\frac{R_{ZCD}\times R_2}{R_{ZCD}+R_2}\left(\frac{VN_{sub}}{V_{ZCD}}-1\right)$$

Since the source current of the ZCD pin input current (absolute maximum rating) is −2.0 mA,+3.0mA the following formula must be satisfied at the same time:

$$R_1>\sqrt{2}\times V_{AC(max)}\times N_{sub} / N_p / I_{SoZCD}$$

where,

I_{SoZCD}: ZCD pin input current (source current = −2.0 mA)

$$R_1>\left(V_{OUT(max)}\times\frac{N_{sub}}{N_s}-7.5\right) / I_{SiZCD}$$

I_{SiZCD}: ZCD pin input current (sink current = +3.0 mA)

V_{OUT}(max): Maximum output voltage

Generally, R1 is around several tens kΩ, whereas C1 is around several tens pF. If timing of bottom detection is OK, C1 need not be connected.

Add Schottky diode between ZCD-GND as shown in Figure 18 when the terminal ZCD input current is not filled even if R1 is appropriately adjusted.

If R1 and C1 constants are not appropriate, overvoltage protection may not function properly. Figure 19 shows the ZCD pin waveform at the time of overvoltage protection. With the upper ZCD pin waveform, overvoltage on the secondary side is detected properly, and latch-off is performed by fault protection. Meanwhile, with the lower ZCD pin waveform, protective function is not operated because the threshold voltage is not reached in 4.5 μs(FA5648:1.0μs). In this case, adjust R1 and C1.

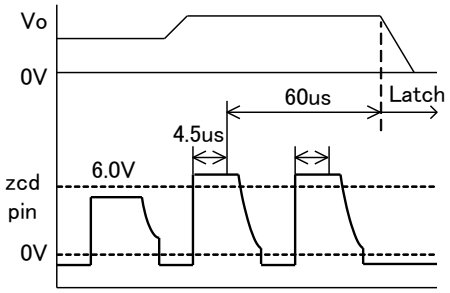


Fig.16 ZCD pin waveform at overvoltage on the secondary side

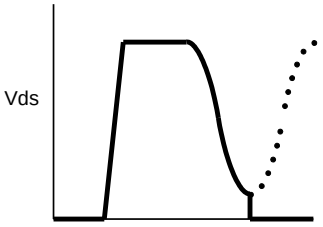


Fig.17 Vds waveform

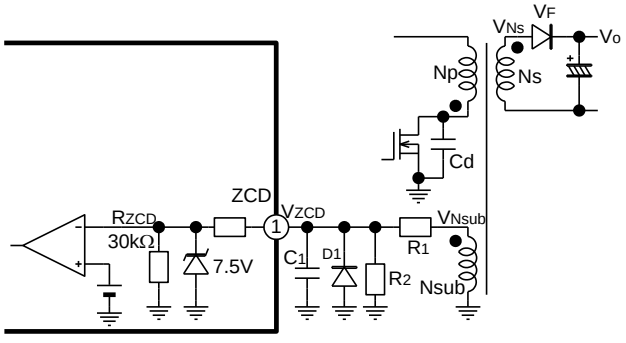


Fig.18 ZCD pin resistance R1 calculation

(2) Pin No. 2 (FB pin)

Function

(i)Input feedback signals from the error amplifier on the secondary side.

(ii)Detects overload status.

(iii)Stops switching for burst operation.

How to use

(i) Feedback signal input

• Connection method

Connect the optocoupler corrector to this pin will allow reguration. At the same time, to prevent generation of noise, connect a capacitor in parallel to the optocoupler (Fig. 20).

• Operation

Pin No. 2 is biased from the IC internal power supply via the resistance. The FB pin voltage is level-shifted and input into the current comparator to provide the threshold voltage of the MOSFET current signals to be detected with the IS pin.

(ii) Overload detection

• Connection method

The same as the feedback signal input in (i).

• Operation

In case of overload, the output voltage decreases to lower than the setting, therefore the FB pin overshoots to the high side. This state is detected to judge overload status. The threshold voltage for overload judgment is 3.5 V.

By the automatic recovery function, overload status brings about hiccup operation, and once the overload state is reset, operation is automatically resumed. See 9. (3) “Operation under overload” for details of operation.

(iii) Stopping switching for burst operation

• Connection method

The same as feedback signal input in (i)

• Operation

FB pin voltage decreases under light load. If this voltage decreases to threshold voltage of stopping on-pulse or lower, switching is stopped, and switching is resumed if the voltage increases to the threshold voltage of stopping on-pulse or higher. By repeating this operation, burst operation is achieved. To undershoot the FB pin voltage significantly at the time of burst operation, the internal FB pin resistance is switched (Fig. 20).

To compensate the dependence of load point for entering burst operation on the high-line voltage, the pulse shutdown FB threshold voltage is switched to 0.35 V for high line voltage, and 0.45 V for low line voltage.

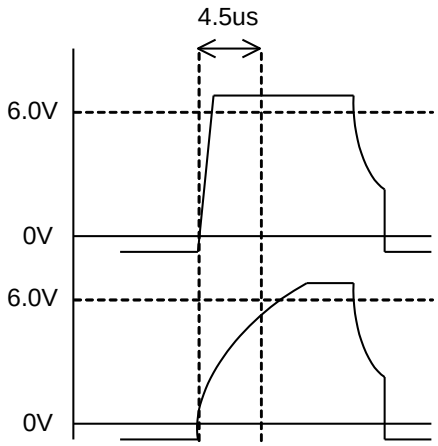


Fig.19 ZCD pin waveform at overvoltage

Advice for designing

The FB pin provides threshold voltage of the current comparator. If noise is added to the pin, output pulse fluctuation may result. To prevent generation of noise, a capacitor having the capacitance of approximately 1000 pF to 0.01 μF is connected for use as shown in Fig. 20.

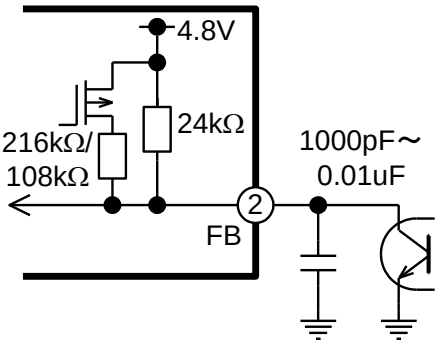


Fig.20 FB pin circuit

(3) Pin No. 3 (IS pin)

Function

(i) Detects and limits the current value of the MOSFET.

(ii) Switches the maximum threshold voltage of current limit by external signals.(Standby mode function) (Except FA5643)

(iii) Detection of transformer short circuit protection

How to use (FA5643)

(i) Current detection and current limiting

• Connection method

Connect a current detecting resistor Rs between the MOSFET source pin and the GND. The current signals of the MOSFET generated in the resistor are input (Fig. 21).

• Operation

The current signals of the MOSFET input to the IS pin is then input to the current comparator, and if it reaches the threshold voltage determined by the FB pin, the MOSFET is turned off. This FB pin voltage fluctuates due to the feedback circuit from the output voltage to control the MOSFET current.

In addition, since the maximum input threshold voltage is also input to the current comparator, the MOSFET current is limited by the current equivalent to this voltage even in an emergency state such as transient state at the time of startup or overload status.

If overload state continues, the latch-off stop is performed by the overload protection function. Generally, the output current value that is stopped in the latch-off mode varies depending on the high-line voltage, and there may be a case in which the higher the line voltage, the larger the output current that is stopped in the latch mode. To compensate the dependency of overload detection level on the line voltage, the maximum input threshold voltage is switched between 0.5 V (low line voltage) and 0.45 V (high line voltage).

(ii) Switching of current limiting maximum threshold voltage by external signals(Standby mode function, Except FA5643)

• Connection method

As shown in Fig. 22, a diode, current limiting resistor, transistor switch, optocoupler, etc. are added between the auxiliary winding and the IS pin.

• Operation

While the MOSFET remains ON, MOSFET current signals are kept input to the IS pin for comparison with the threshold voltage that is determined by the FB pin. With this IC, IS pin voltage level is detected during this OFF period. By increasing the IS pin voltage to 0.55 V, which is the IS pin standby detection voltage, or higher within 2 μs after the MOSFET is turned off, the maximum input threshold voltage of the IS pin is switched. In this case, the detection level is decreased to approximately 1/7 of that of normal operation. But it is necessary to confirm output power in actual power supply unit because the output power may vary with specification of transformer and circuit constant. For example, the power of the power supply is limited in standby mode. Specifically, the maximum input threshold voltage is switched between 0.15 V (low line voltage) and 0.1 V (high line voltage).

If Low signals are input from the external signal, transistor Tr1 and the optocoupler are set to OFF, and transistor Tr2 is brought into continued state, and the IS pin is subjected to the effect of the auxiliary winding voltage. The auxiliary winding voltage remain positive while the MOSFET is set to OFF, and negative while it is set to ON, and thanks to the function of diode D1, the IS pin voltage is increased to positive side only during the period in which the MOSFET remains OFF.

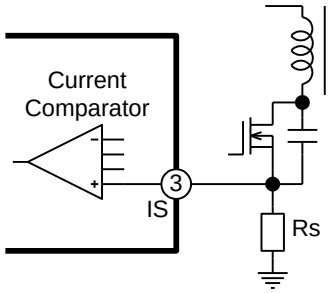


Fig.21 IS pin circuit

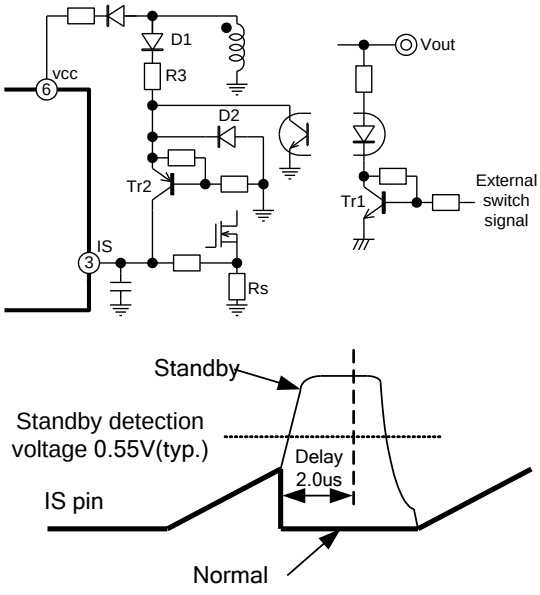


Fig.22 Power limiting circuit and waveform at standby detection

(iii) Detection of transformer short circuit protection

• Connection method (FA5643)

The same as Current detection and current limiting in (i).

• Operation

This IC has function in it that carries out latch shutdown instantly when the voltage higher than 0.97V is impressed to IS pin to protect a transformer short circuit.

This function also carries out instantly latch shutdown except a transformer short circuit when the voltage higher than 0.97V is impressed to IS pin. Therefore if the high voltage is impressed to the input side such as lightning surge, the protection operation may carry out latch shutdown.

In such a case the values of IS pin filter Ris, Cis and a surge protection element for the input line should be readjusted. (See Fig.23.)

Advice for designing

(1) Insertion of a filter

Since this IC has a leading edge blanking (minimum ON width: 290 ns), malfunction due to surge current generated at the MOSFET is switched on does not occur. However, if the surge current generated at the leading edge of OUT is large, or external noise is added, malfunction may occur. In such cases, add a CR filter to the IS pin as shown in Fig. 24.

The filter constant depends on the magnitude of the noise, but as the time constant of Ris × Cis, about 500 ns or less is recommended. Note, however, the overload detection level and the load level of starting burst operation may vary, thus audible noise may be generated or standby power may vary. Pay special attention to the above phenomena.

(2) Burst operation point adjustment 1 under light load

If burst operation is started under heavy load, the audible noise may be generated at transformer. To decrease the burst point slightly, add resistor R4 between the IS pin and the OUT pin (Fig. 25). If R4 is connected, the positive bias voltage is applied to the IS pin voltage when the MOSFET is turned-on, and consequently, the FB pin voltage also remains high level. Since burst operation occurs if the FB pin voltage decrease to 0.45 V (at low line voltage) or lower, burst operation does not tend to occur if the FB pin voltage remains high. Even if a resistor is added between the IS pin and the OUT pin, the effect of resistor R4 may not be obtained if Ris is small. In this case, decrease Cis and increase Ris, while fixing the time constant of the filter (Ris = 470 Ω is recommended when R4 is added).

Note, however, that the standby power may increase, or overload detection level may vary. With this IC, though the dependency of overload detection level on line voltage has been compensated, this ratio may deviate. Confirm there is no problem in application enough.

(3) Burst operation point adjustment 2 under light load

To allow bust operation to occur under slightly heavier load, thus to improvement the efficiency under light load, on condition that there is no transformer audible noise problem, add resistor R5 between the IS pin and the OUT pin (Fig. 26). Note, however, that the overload detection level varies in this case also. With this IC, though the dependency of overload detection level on line voltage has been compensated, this ratio may deviate. Confirm there is no problem in application enough.

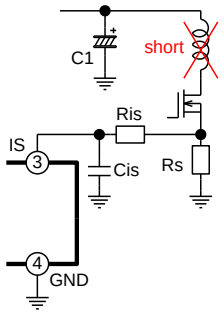


Fig.23 Transformer short circuit protection

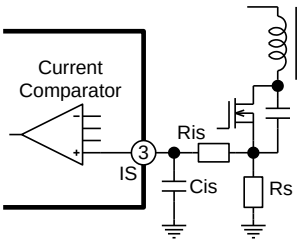


Fig.24 IS pin filter

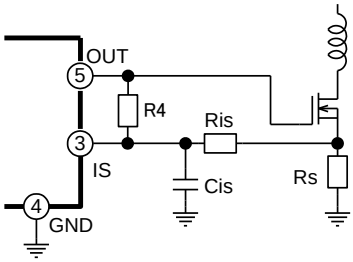


Fig.25 Burst operation point adjustment 1

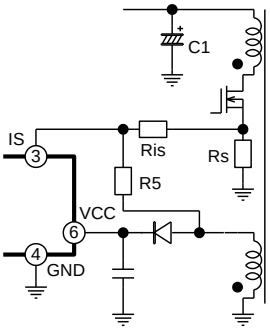


Fig.26 Burst operation point adjustment 2

(4) Switching of current limiting maximum threshold voltage by external signals (Except FA5643/48)

Diodes D1 and D2 in Fig. 22 can share parts with the diode connected between the VCC pin and the auxiliary winding.

While the MOSFET is turned-off, the voltage of auxiliary windings is depended on output voltage on the secondary side and ratio of the number of turns of secondary windings and number of turns of auxiliary windings. As the pull-up level of the IS pin voltage, determine the value of R3 so that the IS pin voltage reaches IS pin standby detection voltage 0.55 V, or higher within 2 μs after the turn OFF. In this case, if Ris is small, the IS pin voltage may not increase. Therefore, adjust the constant of the filter, following the description in (2) “Burst operation point adjustment 1 under light load.”

Diode D2 is added to prevent heating of the MOSFET in the event diode D1 is short-circuited, causing negative voltage to be applied to the IS pin and allowing the ON width to increase abnormally.

(5) Fine adjustment of overload detection level

The overload detection level is determined by the value of resistor Rs in principle. To fine-tune the level, add resistor R6 as shown in Fig. 27 to input the voltage divided by resistors Ris and R6 into the IS pin.

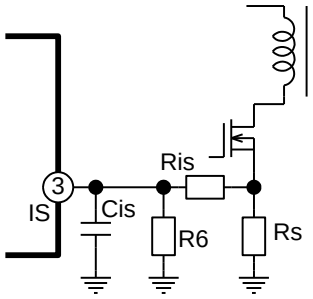


Fig.27 Fine adjustment of overload detection level

(4) Pin No. 4 (GND pin)

Function

Pin No. 4 serves as the basis of the voltage of each part of the IC.

(5) Pin No. 5 (OUT pin)

Function

Drives the MOSFET

How to use

• Connection method

Connect pin No. 5 to the MOSFET gate (Figs. 28, 29, and 30).

• Operation

While the MOSFET remains ON, it is in high state, and VCC voltage is output.

While the MOSFET remains OFF, it is in low state, and 0 voltage is output.

Advice for designing

Connect the gate resistor to limit the current fed to the OUT pin or prevent vibration of gate pin voltage.

Adjust the gate resistor not to exceed the IC output current rating of 0.25 A (source) and 0.5 A (sink).

(6) Pin No. 6 (VCC pin)

Function

Supplies for the IC.

How to use

• Connection method

Generally, the pin is connected the auxiliary winding of the transformer which is rectified and smoothed (Fig. 31).

The auxiliary winding that can be connected to the ZCD pin can be shared.

• Operation

Set the voltage to be supplied from the auxiliary winding within the 11 to 26 V range (recommended operation condition) in normal operation. Since the startup circuit is operated when the VCC pin voltage decreases to the startup current restart voltage, 9 V, or lower, the VCC pin voltage is recommended to be used by 11 V or higher because the startup circuit is not operated.

It is also possible to operate the IC not by using the auxiliary winding but using the current supplied from the startup circuit. However, standby power increases and heating of IC also increases in these cases. Consequently,

to achieve low standby power, it is recommended to supply VCC from the auxiliary winding.

At the same time, if the startup circuit only is used for startup, the MOSFET to be driven must be selected carefully because there is a limit in current to be supplied.

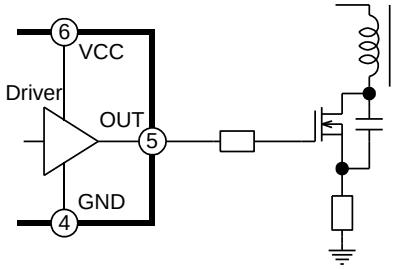


Fig.28 OUT pin circuit (1)

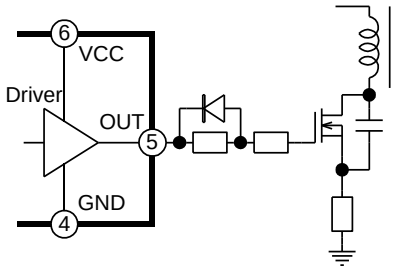


Fig.29 OUT pin circuit (2)

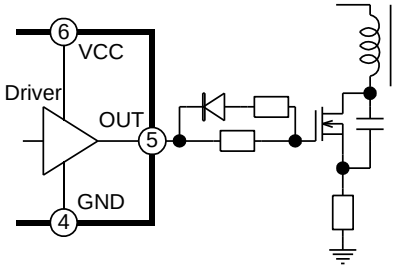


Fig.30 OUT pin circuit (3)

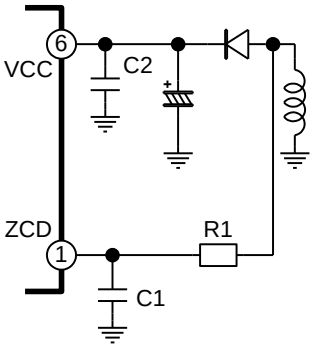


Fig.31 VCC circuit

Advice for designing

(1) Connection of the bypass capacitor

Since large current is fed to the VCC pin when the MOSFET is driven, relatively large noise tends to be generated. In addition, noise is also generated from the current supplied by the auxiliary winding. If this noise is large, malfunction of the IC may result. To minimize the noise that is generated at the VCC pin, add a bypass capacitor C2 (0.1 μF or higher) adjacent to the VCC pin of the IC, between VCC and the GND, as shown in Fig. 31, in addition to the electrolytic capacitor.

(2) Adjustment of power supply voltage input range

The recommended supplied voltage range is 11 V to 26 V. When the load is light, the VCC pin voltage decreases, whereas when the load is heavy, the voltage increases, thus deviating from the power supply voltage range. In such cases, change the resistor between the VCC pin and the diode to adjust the voltage. Also, by adding beads core at the foot of the resistor, voltage fluctuation may be suppressed.

If the above methods do not work, it is recommended to change the secondary winding and the auxiliary winding of the transformer to bifilar winding.

(3) When power is supplied directly to the VCC pin

When directly supplying power to the VCC pin without using VH pin, open the VH pin or short-circuit the VH pin and the VCC pin for use.

If the VH pin is connected to the GND, leakage current may be generated.

(7) Pin No. 7 (N.C.)

Since this pin is placed adjacent to the high-voltage pin, it is not connected to inside the IC.

(8) Pin No. 8 (VH pin)

Function

(i) Supplies startup current.

(ii) Detects and compensates by the high-line voltage. (Except FA5642)

How to use

(i) Supply startup current.

• Connection method

Connect the pin to the high-voltage line. In this case, if connection is to be made after rectification, connect it via a resistor of several kΩ (Fig. 34). On the other hand, if connection is to be made before rectification, connect it to the high-voltage line via a resistor of several kΩ and a diode (Figs. 32 and 33).

• Operation

This IC, which integrates a startup circuit having withstand voltage of 500 V, achieves low power consumption.

Figure 32 presents a typical connection method, in which the VH pin is connected to the half-wave rectification waveform of the AC line voltage. With this method, the startup time is the longest of the three connection methods. In addition, since current supply from the VH pin is interrupted if the AC line voltage is interrupted after the IC enters the latch-off mode, the latch-off mode can be reset in a period of time as short as several seconds.

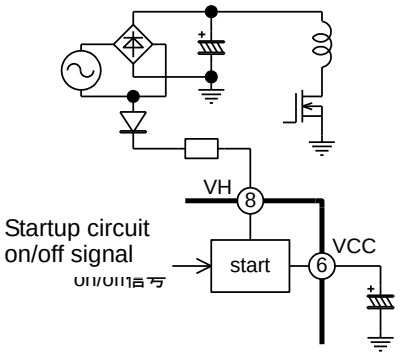


Fig.32 VH pin circuit (1)

With the connection shown in Fig. 33, the VH pin is connected to the full wave rectification waveform of the AC line voltage. The startup time of this method is approximately half of that of the half-wave rectification shown in Fig. 32. In addition, by interrupting the AC line voltage, the time required for resetting the latch mode is as short as the case shown in Fig. 32. But this connection method may malfunction when the model which is integrated line voltage compensation is used, so FA5642 only is recommended this connection.

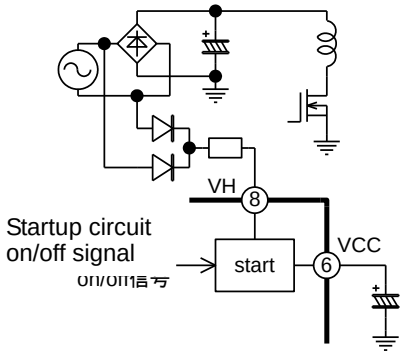


Fig.33 VH pin circuit (2)

With the method shown in Fig. 34, the VH pin is connected after the AC line voltage is rectified and smoothed. The startup time of this method is the shortest of the three connection methods. However, since the voltage charged in the bulk capacitor is applied to the VH pin even if the AC line voltage is interrupted after the IC enters the latch-off mode, longer time is required to reset the latch-off mode. Note that several minutes are required to reset the latch-off mode after the AC line is interrupted, although the duration depends on the operating conditions.

If power is turned on, the capacitor connected to the VCC pin is charged due to the current supplied from the startup circuit to the VCC pin via the VH pin, and the VCC voltage increases. When the ON threshold voltage of 14 V of the low-voltage malfunction prevention circuit (UVLO) is exceeded, the internal supply is started to operate the IC. If VCC is not supplied from the auxiliary winding, the startup circuit is stopped. Meanwhile, if power is not supplied from the auxiliary winding, the current supplied from the startup circuit is used for the normal operation of the IC. If VCC is supplied only from the startup circuit, without the supply from the auxiliary winding, the standby power increases, and the heating of the IC may increase. Consequently, to keep the standby power at low level, it is desirable to supply VCC from the auxiliary winding.
At the same time, if the startup circuit only is used for startup, there is a limit in current to be supplied. Consequently, the MOSFET to be driven must be selected carefully.

The current fed from the VH pin to the VCC pin is approximately 8 mA when VCC = 6.5 V. Note that when VCC = 0 V, the current decreases to 0.7 mA to cope with abnormal state such as short circuit between pins.

(ii) The peak voltage of the line voltage is detected to subject it to high/low line voltage compensation. (Except FA5642)

• Connection method

The same as the method of supplying startup current in (i)

• Operation

If voltage after rectification is input to the VH pin, each threshold level is switched at 226 V when the VH pin voltage is increasing, and 212 V when it is decreasing. If half-wave and full-wave rectification waveforms are input, it is switched at 160 Vrms. The input detection switching delay time is 30 ms.

The threshold level for switching based on input voltage include the pulse shutdown FB voltage, which is related to the burst operation, and the maximum input threshold voltage, which is the overload limit level of the IS pin.

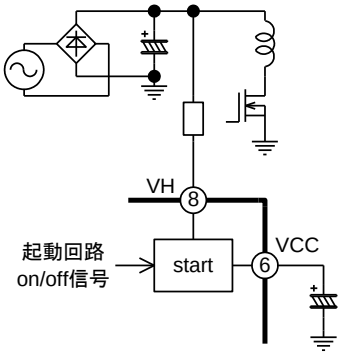


Fig.34 VH pin circuit (3)

Advice for designing

(1) Startup resistor

To prevent damage to the IC due to surge voltage of the AC line, it is recommended to connect a startup resistor whose resistance within the 2 kΩ to 10 kΩ range to the VH pin in series.

Startup time or startup voltage cannot be adjusted using this startup resistor. Note that a resistor having too large resistance may result in inability to startup.

(2) To supply power directly to the VCC pin

To supply power directly to the VCC pin without using a VH pin, open the VH pin or short-circuit the VH and the VCC pins.

If the VH pin is connected to the GND, leakage current may be generated.

(9) Other advice on designing

(1) Surge that occurs at startup due to the minimum switching frequency limiting

Our lineup includes the one that the minimum switching frequency and the maximum ON width are set with this IC to reduce audible noise at the time of starting /stopping. However, due to this minimum switching frequency function, there is a period in which the IC is operated in continuous conduction mode at startup, which may result in increased surge voltage of the diode on the secondary side. Please consider using the one that this minimum switching frequency limiting function was not integrated if the serge of the diode is a problem.

(2) Switching frequency at the time of bottom skip

This IC detects ON/OFF width using the ZCD pin, thus controlling the number of times of bottom skips. Bottom skip is performed up to the point where the IC is turned on at the fourth bottom depending on the load. At this time, depending on the specifications of the power supply or design conditions of the transformer, the switching frequency at the time of bottom skip may be decreased to 40 kHz or lower. If this frequency interferes with other devices, causing problems, for example, adjust the resonance capacitor connected between the drain and the source of the MOSFET. If the capacitance is reduced, the resonance frequency increases, allowing the switching frequency at bottom skip to increase.

(3) Preventing malfunction due to negative voltage of the pin

If large negative voltage is applied to each pin of the IC, the parasitic devices within the IC may be operated, thus causing malfunction. Confirm that the voltage of -0.3 V or less is not applied to each pin.

The vibration of the voltage generated after the MOSFET is turned-off may be applied to the OUT pin through the parasitic capacitance, resulting in a case in which negative voltage is applied to the OUT pin.

In addition, negative voltage may be applied to the IS pin due to the vibration of surge current generated at the turn-on of the MOSFET.

In such cases, connect a Schottky diode between each pin and the GND. The forward voltage of the Schottky diode can suppress the negative voltage at each pin. In this case, use a Schottky diode whose forward voltage is low. Figure 35 is a typical connection diagram where a Schottky diode is connected to the OUT pin.

(4) Loss calculation

To use the IC within its rating, it is necessary to confirm the loss of the IC. However, since it is difficult to measure the loss directly, the method of confirming the loss by calculation is shown below. If the voltage applied to the VH pin is defined as VVH, the current fed to the VH pin during operation as IVHrun, power supply voltage as VCC, supply current as Iccop1, gate input charge of the MOSFET to be used as Qg, and switching frequency as fsw, the total loss Pd of the IC can be calculated using the following formula.

$$P_d \approx V_{CC} \times (ICC_{op1} + Q_g \times f_{sw}) + V_{vh} \times IVH_{run}$$

A rough value can be found using the above formula, but note that Pd is slightly larger than the actual loss value. Also note that each specific characteristic value has temperature characteristics or variation.

Example:

If the VH pin is connected to a half-wave rectification waveform with AC 100 V input, the average voltage to be applied to the VH pin is approximately 45 V. In this state, assume that VCC = 15 V, Qg = 80 nC, and fsw = 60 kHz (when Tj = 25°C). Since IVHrun = 30 μA and Iccop1 = 0.85mA from the specifications, the standard IC loss can be calculated as follows:

Pd ≈ 15V x (0.85mA + 80nC x 60kHz) + 45V x 30μA ≈ 86.1mW

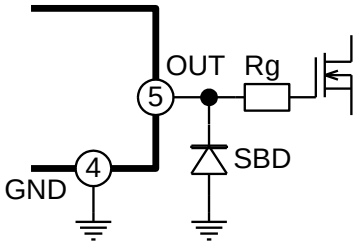


Fig.35 Negative charge prevention circuit

11. Precautions for pattern design

(1) Precautions for pattern design

In order to prevent the malfunction of the control IC (unstable voltage, unstable waveform, latch-off, etc.) caused by the surge voltage (noise) when a current is applied to the pattern on the minus side because of a principal current, a lightning surge test, an AC line surge test, and a static electricity test, consider the following contents when designing the pattern.

The power supply has the following current paths:

1) A principal current applied from the electrolytic capacitor to the primary winding of the transformer, the MOSFET, and the current sensing resistor after AC power supply rectification

2) A rectified current applied from the auxiliary winding of the transformer to the electrolytic capacitor; a drive current applied from the electrolytic capacitor to the control IC and the MOSFET gate.

3) A control current of the control IC for output feedback or the like

4) Filter and surge currents applied between the primary and secondary sides

▪ Separate the patterns on the minus side in 1) to 4) to avoid interference from each other.

▪ To reduce the surge voltage of the MOSFET, minimize the loop of the principal current path.

▪ Install the electrolytic and film capacitors between the VCC pin and the GND in a closest position to each pin in order to connect them at the shortest distance.

▪ Install the filter capacitors for the FB, IS, and ZCD pins and the like in a closest position to each pin in order to connect them at the shortest distance. Especially, connect the patterns on the negative side of the FB and IS pins to the GND pin of the IC, separately from other patterns, keeping the wiring as short as possible.

▪ Avoid installing the control circuit and pattern with high impedance directly below the transformer.

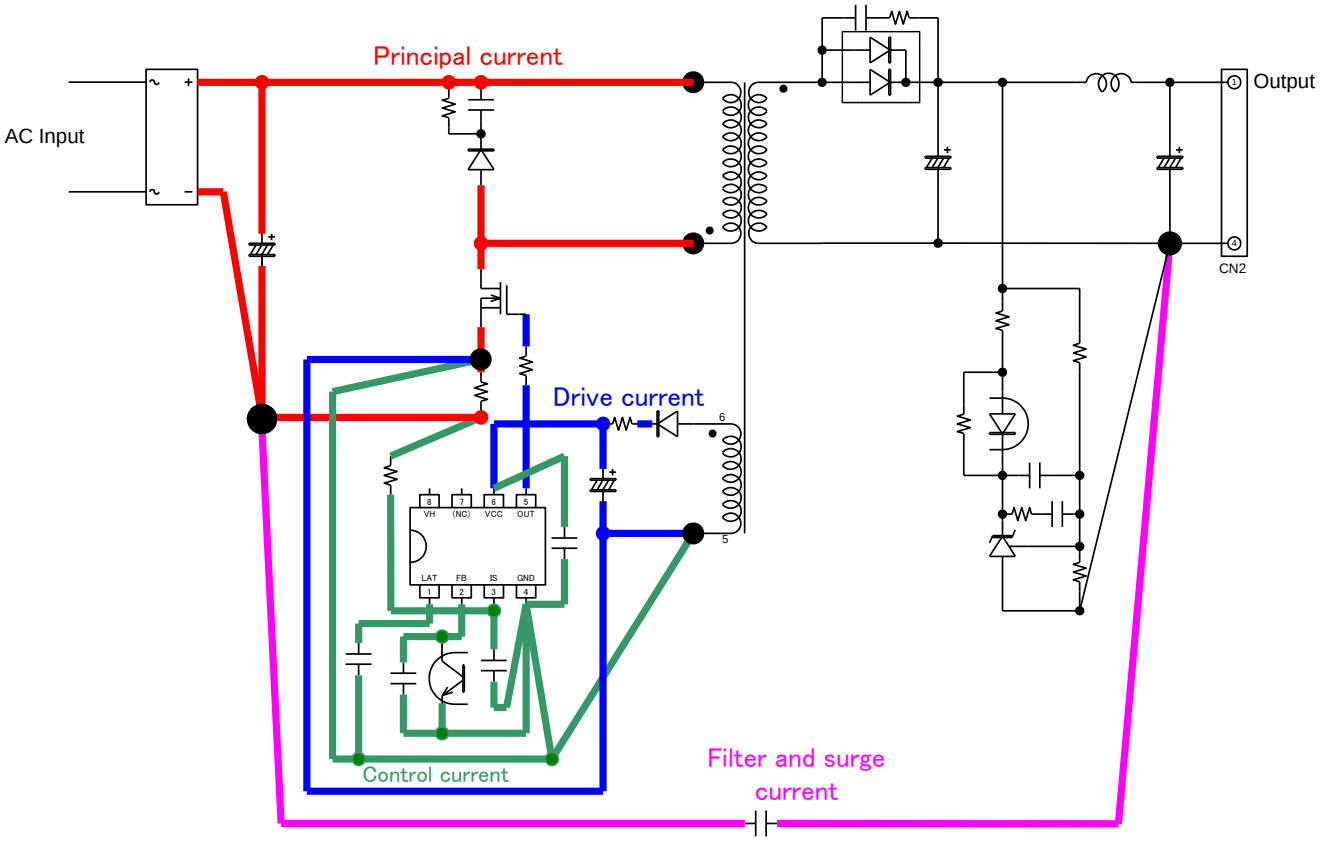
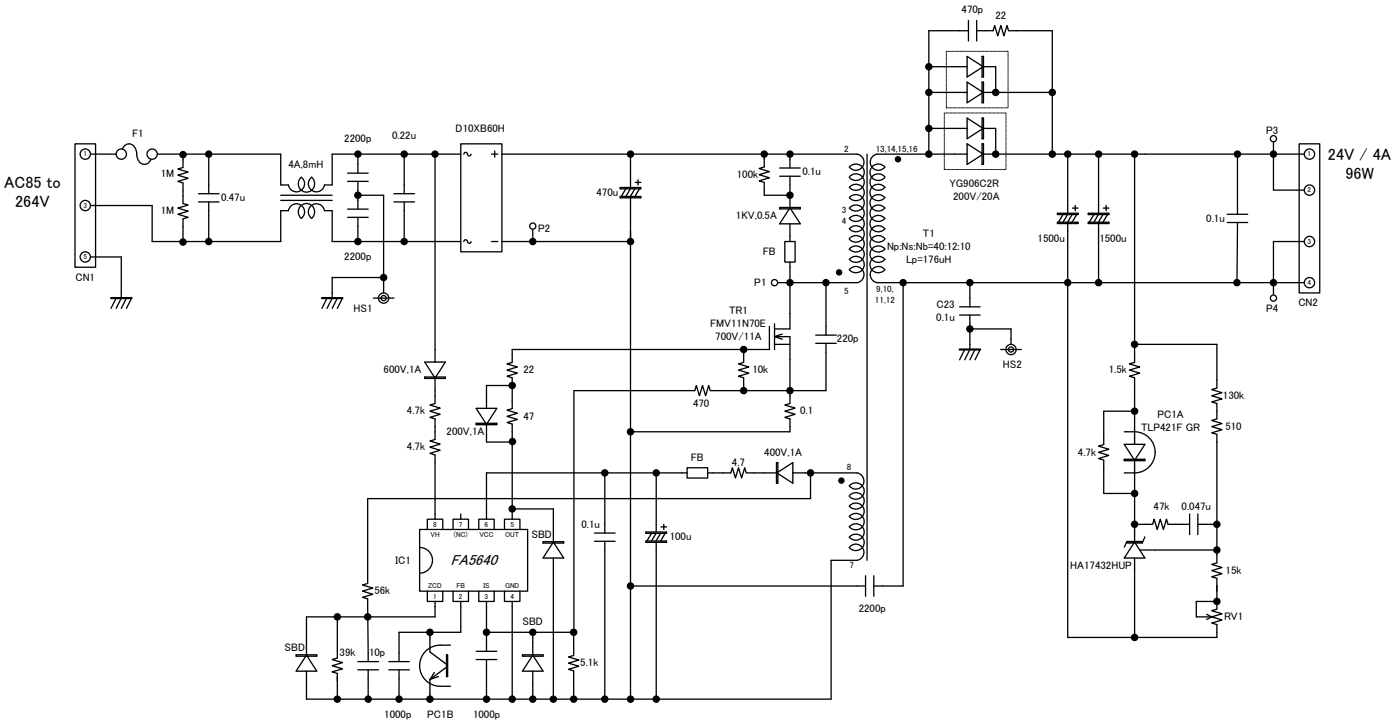


Fig.36 Pattern design image

12. Example of application circuit

The typical application circuit shown here provides specifications common to each IC series.



Note: This application circuit is a reference material for describing typical usage of this IC, and does not guarantee the operation or characteristics of the IC.