

FUJI Power Supply Control IC

DC/DC Power Supply control IC

FA7764

Application Note

June-2010
Fuji Electric Systems Co.,Ltd

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Notices:

- The specifications in this document are subject to change without notice.
- Parts tolerance and characteristics are not defined in all application described in this Data book. When design an actual circuit for a product, you must determine parts tolerances and characteristics for safe and stable operation.

1. Overview

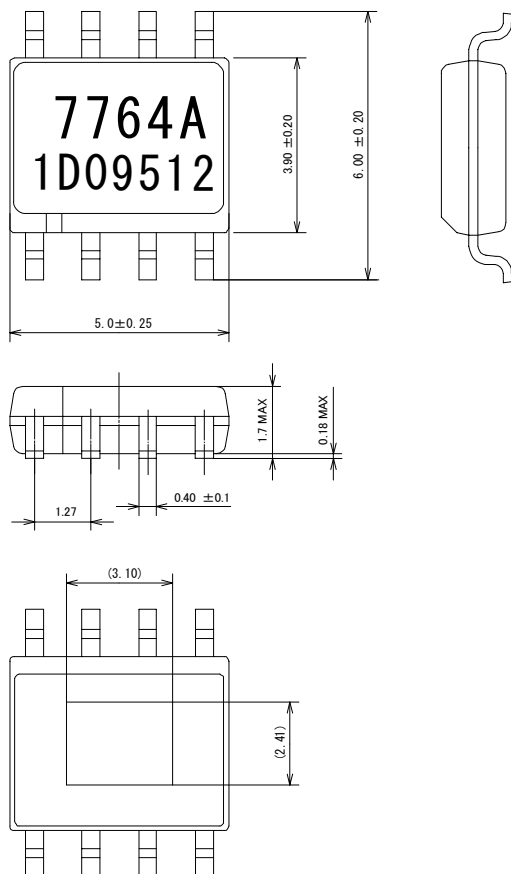
The FA7764N is a single output step-down DC-DC converter with built-in power MOSFET. Featuring a high voltage process, it is suitable for the DC-DC converter with input voltages of up to 45 V and output currents of up to 1.5 A. It operates with the current mode control and also it can reduce external parts. Furthermore it achieves a fast response. The circuit protections are built-in to achieve safety power supply circuit.

2. Features

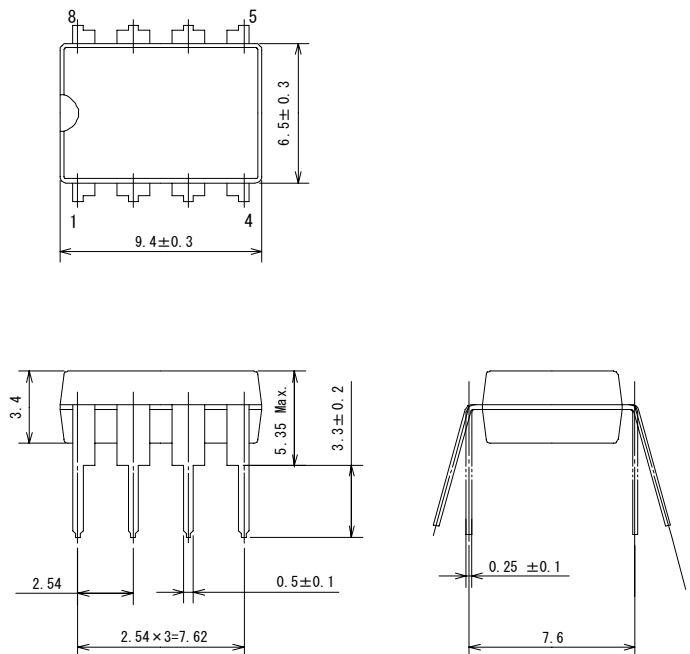
- Single output with the built-in power MOSFET.
- High efficiency 85% at 24V input and 5 V/1.2 A output with 200kHz operation.
- Stable operation with current mode control.
- Switching frequency selectable from 30 kHz to 400 kHz.
- ON/OFF function: Current consumption 0.1mA(max.) at OFF mode.
- Current consumption of the VCC terminal during operation is 0.5mA(typ.).
- Protection functions:
 - Over current limitation for the power MOSFET
 - Soft start (8 ms)
 - Short-circuit protection with the timer and latch (90ms delay time)
 - Thermal shut down
 - Protection for opened rectifier diode
- SOP-8pin package with the exposed pad.

3. Outline

•FA7764AN(SOP-8 E-Pad)

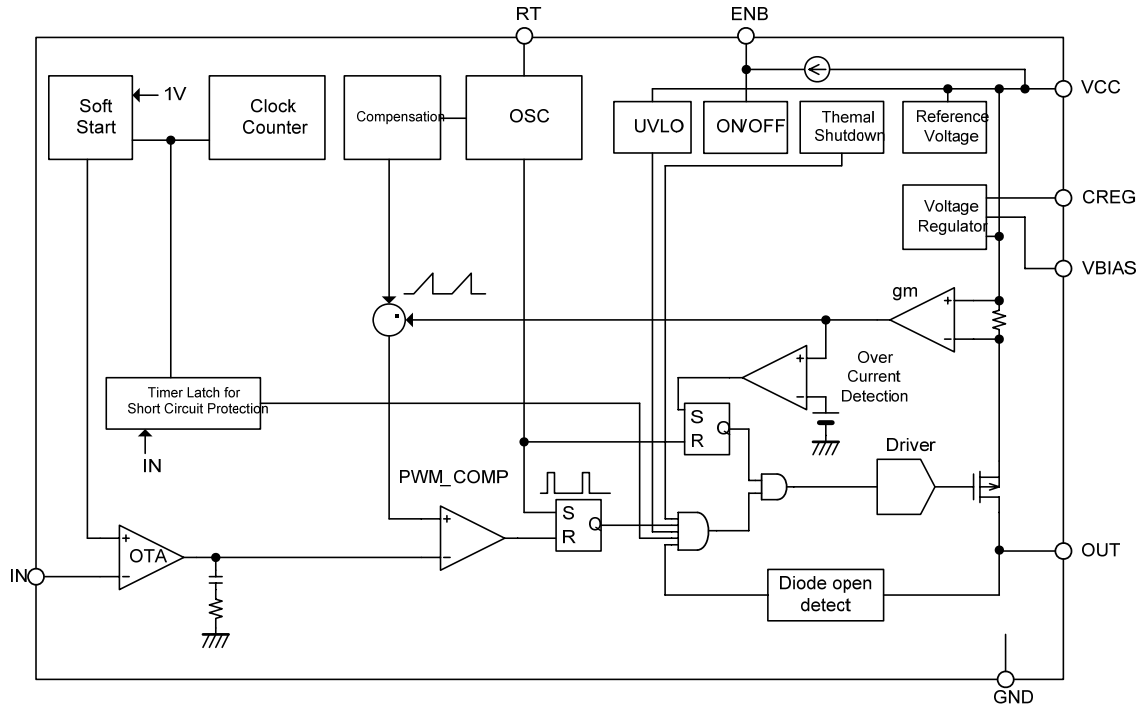


•FA7764P(DIP-8)



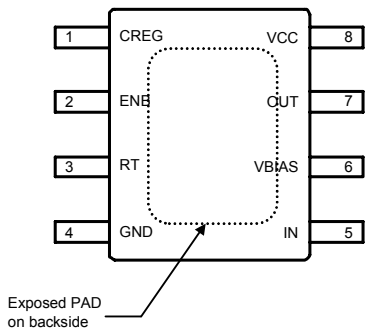
Units : mm

4. Block diagram

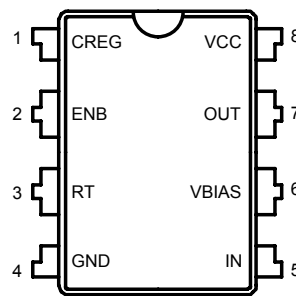


5. Description of the terminal functions

FA7764AN(SOP-8 E-Pad)



FA7764P(DIP-8)



Terminal No.	Terminal code	Terminal function	Remarks
1	CREG	Internal power supply output	Connect stabilization capacitor
2	ENB	ON/OFF control (L, operation; H or open; standby mode)	
3	RT	Timing resistor for the oscillator	
4	GND	Ground	
5	IN	Inverted input of error amplifier	
6	VBIAS	Voltage input for internal power supply VBIAS = up to 3.1 V; CREG is powered by VCC. VBIAS: 3.1 V or more; CREG is powered by output voltage.	Supply from output voltage
7	OUT	Switching output	
8	VCC	Power supply input	Connect bypass capacitor

6. Ratings and characteristics

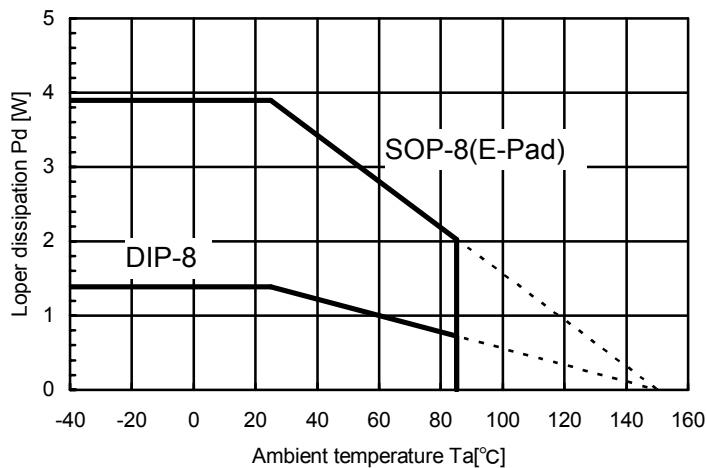
(1) Absolute maximum rating

Following data are subject to change without notice. When using this IC, be sure to obtain the latest specifications.

*The items except operation junction temperature, operating ambient temperature, and storage temperature.

Item	Symbol	Condition	Rating	Units
Power Supply voltage (VCC)	V _{CC}		50	V
IN input voltage	V _{VIN}		-0.3 to 4.0	V
CREG input voltage	V _{CREG}		-0.3 to 4.0	V
RT input voltage	V _{RT}		-0.3 to 4.0	V
VBIAS input voltage	V _{VBIAS}		-0.3 to 6.0	V
ENB input voltage	V _{ENB}		-0.3 to 4.0	V
Power dissipation *1	SP-8(E-Pad)	Ta ≤ 25°C	3.9	W
	DIP-8		1.39	
Operation junction temperature	T _J		+150	°C
Operation ambient temperature	T _{OPR}		-40 to +85	°C
Storage temperature	T _{STG}		-50 to +150	°C

The characteristic of power dissipation



*1 This IC should be used less than the total power dissipation (Pd). This Pd is based on the condition that this IC is mounted on 4-multi-layer PCB(the size is 50mm×40mm) and the Exposed pad (E-pad, in the reverse side of the IC package) is connected to the ground at Ta=25 degrees.

Over 25 degrees, delating the Pd as follows:

Thermal resistance	θ _{j-a} (Junction to Ambient)	SOP-8(E-Pad):32 degrees/W, DIP-8:95 degree/W
	θ _{j-c} (Junction to Case)	SOP-8(E-Pad):16.5 degrees/W, DIP-8:55 degree/W
	θ _{EPAD-c} (E-pad to Case)	SOP-8(E-Pad):6 degrees/W

Note) This IC should be used on the condition that the junction temperature is less than 150 degrees, based on the total power dissipation.

Also this IC should be examined that the junction temperature is actually less than 150degrees by measuring the surface temperature of this package.

(2) Recommended operating conditions

Item	Symbol	Condition	MN.	TYP.	MAX.	Units
Power Supply voltage (VCC)	V_{CC}		9		45	V
VBIAS input voltage	V_{VBIAS}		3.1		5.5	V
Oscillation frequency	f_{OSC}		30		400	kHz
CREG pin capacitance	C_{REG}		0.1	-	-	μF
VBIAS pin capacitance	C_{VBIAS}		-	0.1	-	μF

(3) Electrical Characteristic

- The characteristics is based on the condition of $V_{CC}=42V, C_{REG}=0.1\mu F, R_T=39k\Omega, T_a=+25^\circ C$, unless otherwise specified.
- Line regulation is the difference from 9V to 45V.

(1)Output feedback voltage (IN,VBIAS pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Feedback reference voltage	V_{IN}		0.990	1.000	1.010	V
Variation with temperature	V_{INdT}	$T_a=-40$ to $+85^\circ C$			± 1	%
Input pin current	I_{IN}	$V_{IN}=0$ to $2V$	-0.15		0.15	μA

(2)Regulated voltage for internal blocks (CREG pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Regulated voltage	V_{REG}	*2	2.6	3.0		V

*2 CREG pin occurs over shoot voltage until about 4V in case of starting by ENB pin.

(3)Oscillator section (RT pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Oscillation frequency	f_{OSC}	$R_T=39k\Omega$	108	120	132	kHz
Line regulation	f_{dV}	$V_{CC}=9V$ to $45V$		± 3	± 5	%
Variation with temperature	f_{dT}	$T_a=-40$ to $+85^\circ C$		± 3	± 5	%

(4)Soft start section						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Soft start time	t_s	*4	4	8	12	ms

*4 t_s is the time of output voltage change from 10% to 90%

(5)Timer and latch for short circuit protection (CP pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Delay time of timer latch	t_{prot}	$V_{CC}=10V$	45	90	180	ms
IN pin on threshold voltage	V_{THINON}	$V_{CC}=10V$ *5-1	0.70	0.75	0.80	V
IN pin off threshold voltage	$V_{THINOFF}$	*5-2,5-3		0.85		V
IN pin Hysteresis voltage	$V_{THINHYS}$	*5-3		0.10		V

*5-1 The counter of timer latch starts when IN pin voltage is lower than V_{THINON} ,

*5-2 The counter of timer latch stops when IN pin voltage is higher than $V_{THINOFF}$.

*5-3 Design value.

(6)Under voltage lockout circuit section (VCC pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
ON threshold voltage	V_{UVLOON}	IC is enabled.		6.9	8.2	V
OFF threshold voltage	V_{UVLOFF}	IC is disabled.	4.9	5.9		V
Hysteresis voltage	$V_{UVLOHYS}$		0.4	1.0		V

(7)ON/OFF control section (ENB pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Source current of ENB	I_{ENB}	$V_{ENB}=0V$		10	15	μA
ON threshold voltage	V_{ENBON}	IC is enabled			1	V
OFF threshold voltage	V_{ENBOFF}	IC is disabled *7	2			V

*7 External voltage input is not necessary to the ENB pin because it clamps to the self-limited voltage near 5V.

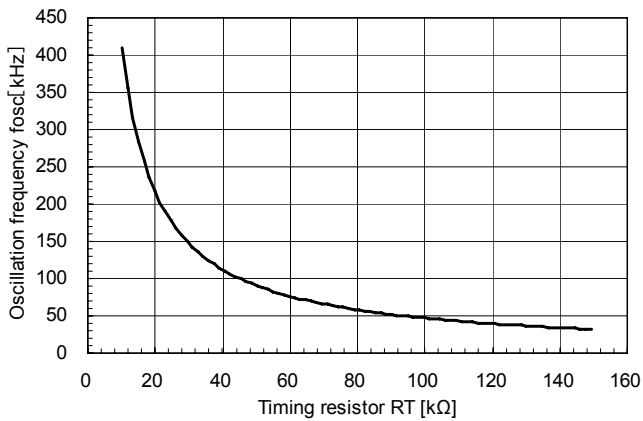
(8)Thermal shutdown section						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Thermal shutdown enable	T_{OHPON}	Output is disabled	125	135		$^{\circ}C$
Thermal shutdown disable	T_{OHPON}	Output is enabled		115		$^{\circ}C$

(9)Output section (OUT pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
On resistance of built-in P-channel MOSFET	R_{ONP}	$V_{CC}=10V, I_{DS}=1.0A$		0.8	1.0	Ω
		$T_a=85^{\circ}C$ $V_{CC}=10V, I_{DS}=1.0A$		1.2	1.5	Ω
Current limit	I_{OLMT12}	$V_{CC}=12V$	2.3	3.0	3.7	A
	I_{OLMT42}	$V_{CC}=42V$	2.5	3.5	5.0	A
Short circuit detect current	I_{OSH}	$V_{CC}=42V$	4.0	6.0	8.5	A
Open diode detect voltage	V_{DOP}		-10	-9	-8	V
Maximum duty limit	D_{MAX}			95		%

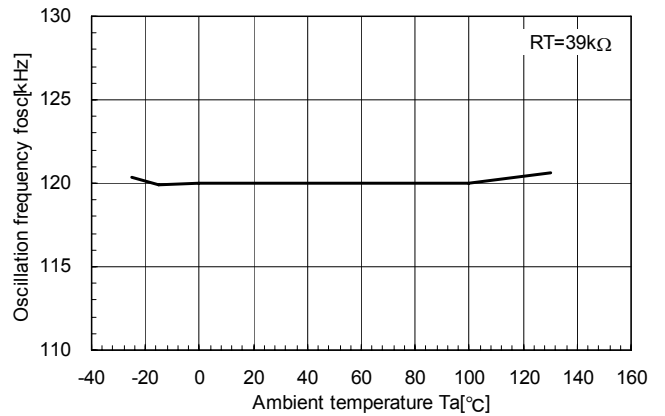
(10)Overall section (VCC,VBIAS pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Supply current (VCC)	I_{CCVCC}	Switching at non-load (at VBIAS<3.1V)		0.85	1.5	mA
		Switching at non-load (at VBIAS>3.1V)		0.5	1.0	
	$I_{CCSTBVCC}$	Stand by (ENB=open)			50	100
Supply current (VBIAS)	$I_{CCVBIAS}$	Switching at non-load (at VBIAS<3.1V)		0	20	μA
		Switching at non-load (at VBIAS>3.1V)		0.5	0.8	mA
	$I_{CCSTBVBIAS}$	Stand by (ENB=open)			0	20

7. Characteristic curves

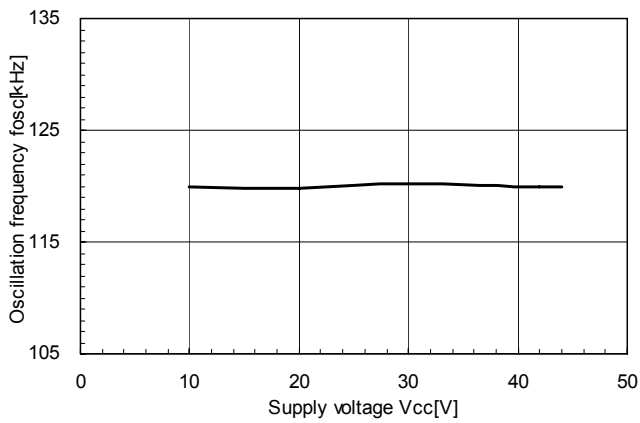
Timing resistor vs. Oscillation frequency



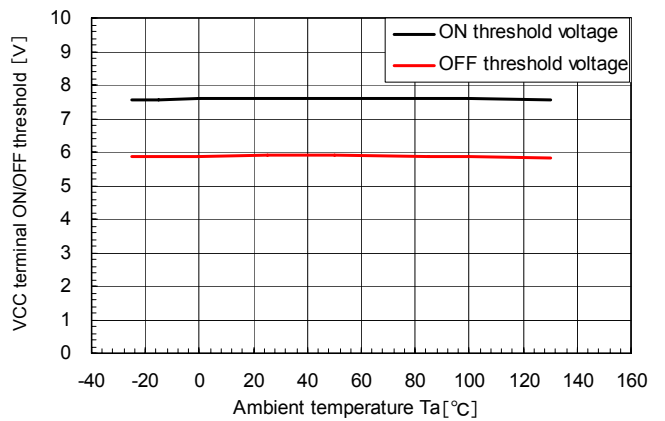
Oscillation frequency vs. ambient temperature



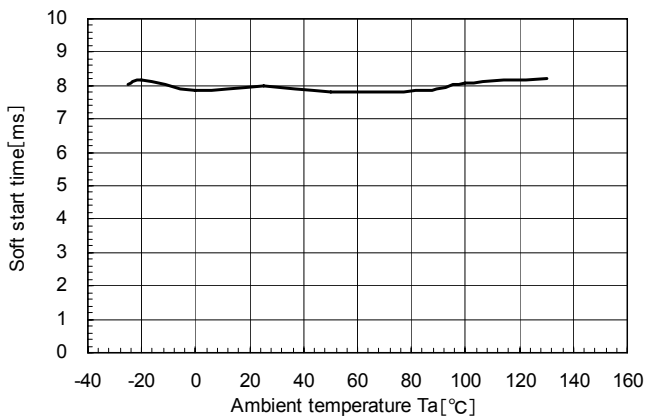
Oscillation frequency vs. Supply voltage VCC



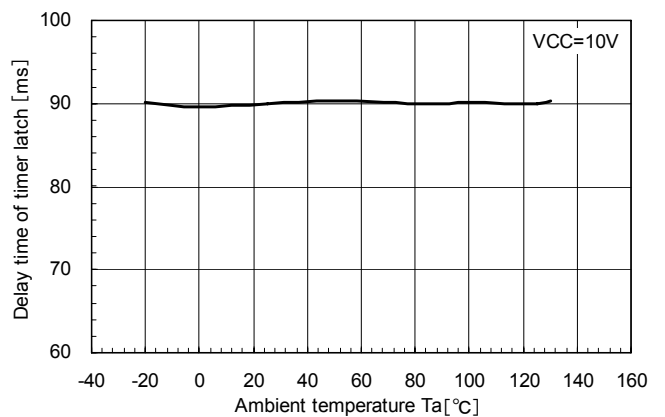
Under voltage lockout vs. Ambient temperature

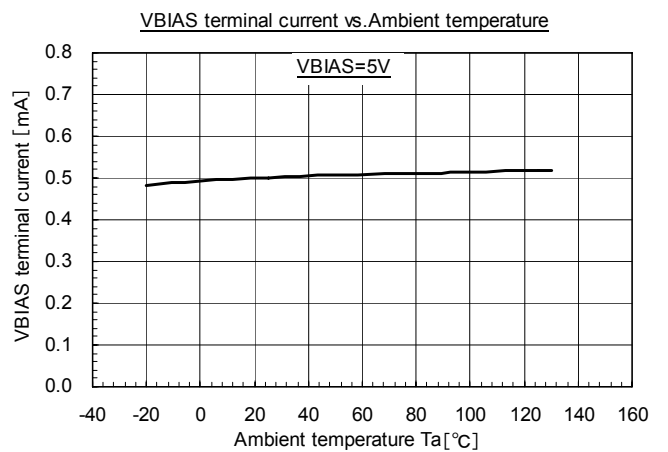
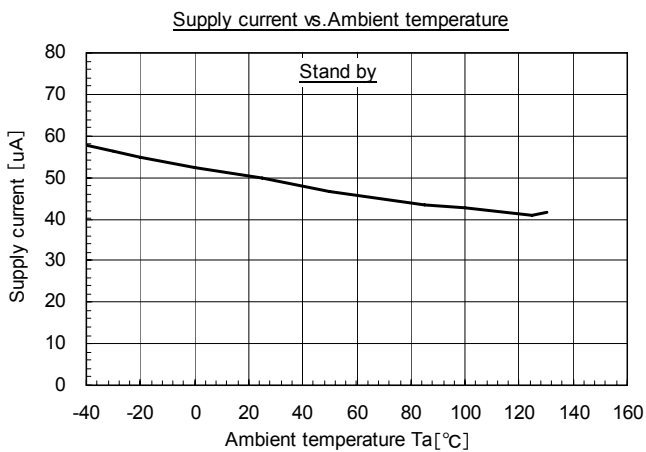
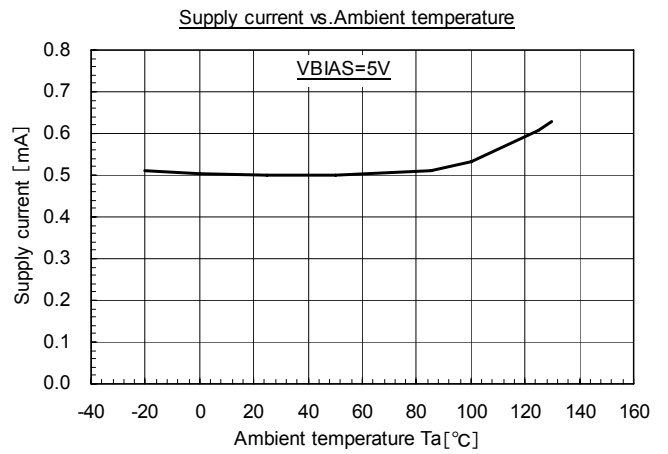
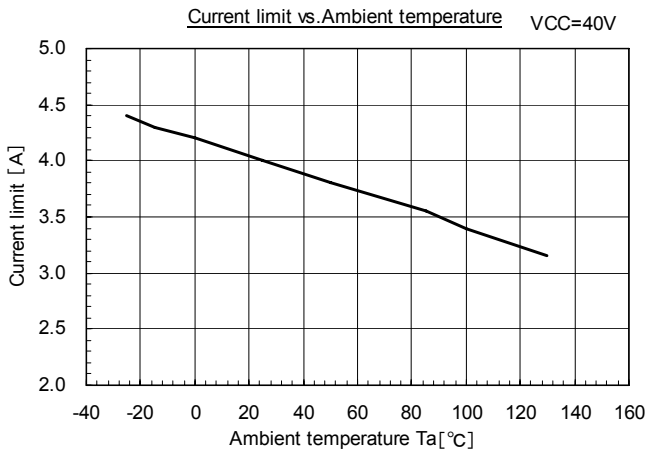
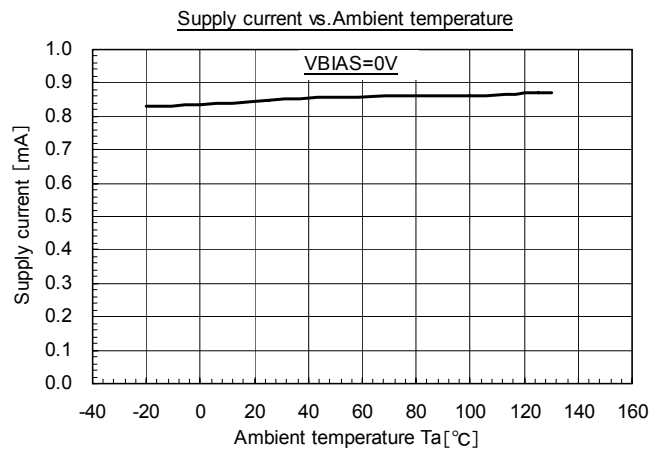
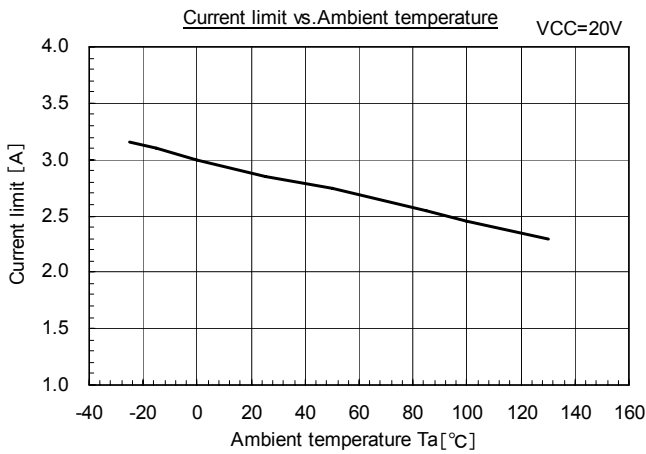


Soft start time vs. Ambient temperature

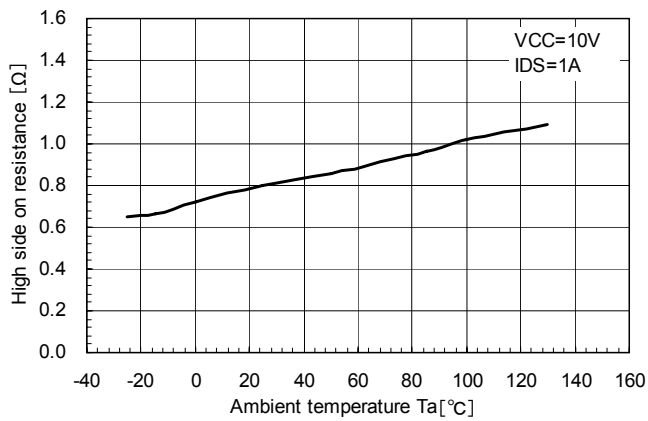


Delay time of timer latch vs. Ambient temperature

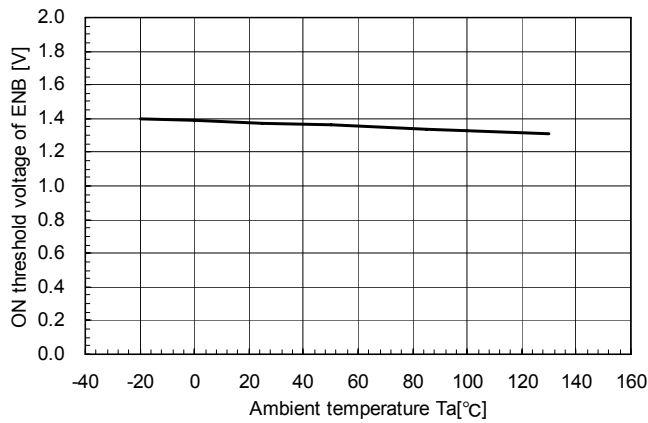




High side on resistance vs.Ambient temperature



ON threshold voltage of ENB vs.Ambient temperature



8. Operation description of each block

(1) Reference voltage circuit

The reference voltage circuit generates the feed back voltage reference (VIN) of 1.00V±1% which compensated in temperature from VCC voltage, and the regulated voltage (CREG) of 3.0V

The feedback voltage (VIN) is connected to the non-inverting input of error amplifier (OTA) as a reference voltage of the error amplifier.

The regulated voltage (CREG) is provided as a regulated power supply for IC's internal blocks, and it has to connect capacitors in order to stabilize voltages.

The CREG voltage is designed specifically for the power supply for IC's internal blocks. Therefore it cannot be used as external stabilized power supplies.

To determine capacitance of CREG pin, refer to recommended operating conditions.

(2) Oscillator

The oscillator generates a triangular waveform by charging and discharging the capacitor.

Oscillation frequency can be set by the value of resistor connected to the RT pin (Fig.1)

(Operating frequency decreases when RT increases, Operating frequency increases when RT decreases)

Set the oscillation frequency between 30 kHz and 400 kHz. The RT pin outputs DC voltage of 1 V.

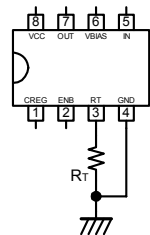


Fig.1

(3) Error amplifier (OTA)

The IN pin (5 pin) is the inverting input of the error amplifier (OTA). The non-inverting input is internally connected to the feedback reference voltage (VIN) with 1.0 V ± 1%. The output of OTA has no external pin and the phase compensations are built-in.

The feedback voltage of the DC-DC converter's output is connected to the IN pin by the divider resistor. The output voltage Vout of the DC-DC converter can be calculated as follows;

$$V_{out} = \frac{R1 + R2}{R2} \times V_{IN}$$

If it operates without stability, connect the capacitor C1 in order to adjust the phase compensation.

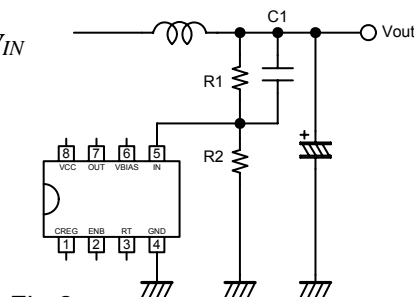


Fig.2

(4) PWM comparator

The ON state of output (at the OUT pin) starts with the ON trigger signal of the oscillator. It turns off when the inductor current reaches to the specified level by the error amplifier (OTA) output.

(5) Soft start circuit

In order to prevent the abnormal start up of DC-DC converter such as rush current, the soft start circuit is built-in.

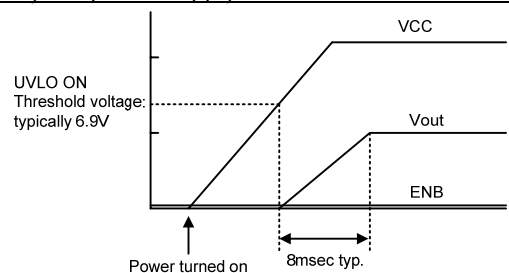
The soft start is performed by raising the feedback reference voltage of the error amplifier (OTA) step by step. Therefore the output voltage of DC-DC converter rises slowly.

The soft start time is fixed to 8msec (typ.) internally.

The soft start starts after the input voltage reaches the ON threshold (6.9V typ.) or more of under voltage lock out (UVLO). (Fig. 3).

In power supplied condition, the soft start is controlled by the ENB signal.

Start up by the power supply with the low level ENB signal



Startup by the ENB signal

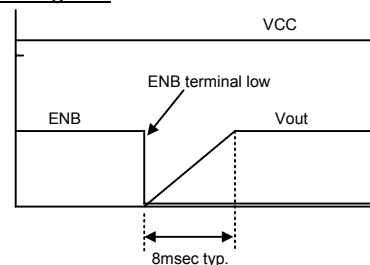


Fig. 3

(6) Timer and latch for short circuit protection

When the output voltage of the DC-DC converter drops continues in constant time, the timer and latch short circuit protection stops switching operation in order to protect the DC-DC converter.

If the output voltage of DC-DC converter drops due to output short-circuit or over load, the output voltage feedback IN pin of the error amplifier will also decrease. When the IN pin voltage drops down to 0.75V (typ.), the timer latch starts its counter.

If the drops continues and the counter operates beyond delay time (90msec typ.), the protection circuit regards the case as abnormal. Therefore it stops switching, and protect the circuit (Fig. 4).

The delay time of the timer and latch is fixed internally and cannot be configured from outside.

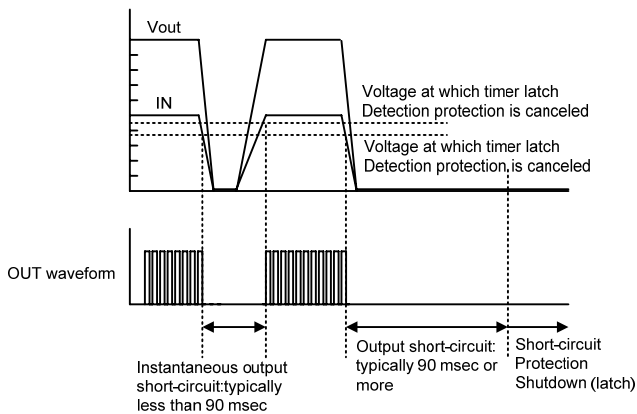


Fig. 4

In order to resetting from latch stoppage, resetting by using the ENB pin or setting the input voltage down to the UVLO threshold voltage are required.

(7) Overcurrent limitation circuit

This IC has a pulse-by-pulse overcurrent limitation function that detects and limits each peak current of the built-in MOSFET.

The current of the built-in MOSFET is transferred to the voltage signal at current detect circuit, and the voltage signal is input into the overcurrent limitation comparator.

If the current transferred voltage signal is higher than the reference voltage, the built-in MOSFET is turned off and the current is limited.

The current limitation will be reset in the next switching period, and it will be repeated in each period along with overcurrent limitation.

Furthermore, when the pulse-by-pulse overcurrent limitation continues for five times, the IC latch stops the switching in order to avoid inductor saturation and the destruction of the MOSFET.

If the output voltage of the DC-DC converter drops to a level lower than 75% (typ) due to line impedance or some other factor, the IC will be shut down by the same way as timer latch short-circuit protection described in (6).

(8) Thermal shut down circuit

The IC has an thermal shut down function that stops switching operation when the IC overheats due to overcurrent or other error.

The IC stops switching when the chip temperature is heated up to 135 degrees (typ.), and the IC resumes switching when the chip temperature is cooled down to 115 degrees.

The latching function does not work when thermal shut down is operated.

(9) ON/OFF controller

This IC can be on/off controlled by the input of external signals to the ENB pin.

To turn the output on, set the ENB pin voltage less than 1.0V. Then the output voltage gradually increases by the soft start (Fig. 3).

The output can be turned off by either opening the ENB pin or input an external voltage of at least 2V. When the ENB pin is open, the ENB pin voltage will clamp to the self-limited voltage near 5V. In this case, the IC keeps standby mode where the regulated voltage CREG (3.0V typ.) is shut down, and also the current consumption of the IC is controlled less than 100 μA(typ.).

(10) Under voltage lockout circuit (UVLO)

This IC has a UVLO function to prevent circuit malfunction in case of a lower input power supply.

When increasing the power supply voltage Vcc from 0V, the IC will be start operation over 6.9V (typ).

When decreasing the power supply voltage Vcc from operation state, the IC will be shut down under 5.9V (typ).

(11) Output circuit

The output circuit consists of P-channel MOSFET, with ON resistance of 0.8 Ω (typically).

(12) Opened rectifier diode protection

Generally when a rectifier diode in the buck converter is removed by some kind of abnormality states, large voltage occurs on switching MOSFET by the energy of the inductor and it has a possibility of destruction the MOSFET with emitting smoke and ignition.

Therefore, the IC will shut down the operation when the OUT pin voltage falls under -9V with synchronized switching.

(13) VBIAS circuit

This IC provides the VBIAS pin to increase the efficiency of the power supply circuit and reduce the IC power loss.

The internal regulated power supply CREG is usually generated by the VCC voltage.

If CREG is generated from the output voltage of the DC-DC converter by the VBIAS pin, it is able to reduce the power loss at CREG regulator and lower power consumption operation (Fig. 5).

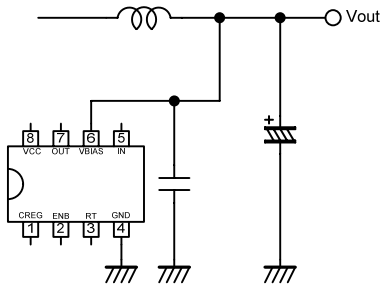


Fig. 5

When the VBIAS pin is not used, the operating current consumption of the VCC terminal is 0.75 mA (typ), on the other hand, when the VBIAS pin is used, the comparable consumption is 0.4 mA(typ).

This operation switchover is performed at the VBIAS pin voltage (i.e., output voltage of the DC-DC converter) of 3.1V. Therefore, the VBIAS operation will be effective only at the input voltage more than 3.1V.

Furthermore, a 5.5 V Zener diode for protection is connected to the VBIAS pin. Therefore, if more than 5.5V voltage is applied to the VBIAS pin, a leak current will be occurred in the Zener diode and also increases the power loss.

Therefore, apply the voltage from 3.1V to 5.5V to the VBIAS pin when you use the VBIAS pin function.

Connect a ceramic capacitor close to the VBIAS pin as shown in Fig. 5 to eliminate noise. The recommended value of the capacitance is about 0.1 μF.

If you do not use the VBIAS pin and in case of set the DC-DC converter output voltage to less than 3.1V or more than 5.5V, connect the VBIAS pin to the GND (Fig. 6).

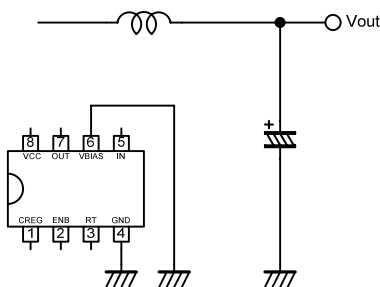


Fig. 6

9. Design tips

(1) Setting an oscillation frequency

The oscillation frequency can be adjusted by changing the value of the resistor connected to the RT pin as described under item (2) in "Operation description of each block." you can set any oscillation frequency between 30 kHz and 400 kHz.

The oscillation frequency can be determined by the characteristic curve of "Timing resistor vs. Oscillation frequency" or the RT value can be approximately calculated as follows:

$$f_{osc} = 3738 \times R_T^{-0.95}$$

Where, f_{osc} : Oscillation frequency [kHz]
 R_T : Timing resistance [kΩ]

This expression, however, can be used as rough calculation, the obtained value is not guaranteed. The operation frequency varies due to the conditions such as tolerance of the characteristics of the ICs, influence of noises, or external discrete components. When determining the values, examine the effectiveness of the values in an actual circuit.

The timing resistor R_T should be connected to the GND pin as shortly as possible because the RT pin is high impedance pin and is easy affected by noises.

(2) IC losses

This IC incorporates a switching MOSFET. The loss generated in this MOSFET accounts for most of the IC loss, and the loss is determined by the input/output conditions of the DC-DC converter.

Attention is needed to the permissible loss of the IC (SOP-8 E-Pad: 3.9 W at 25°C).

The permissible loss in SOP-8 (E-Pad) specified in this document is under the condition of mounting a 4-layer board (50 mm x 40 mm) at T_a of 25°C when the exposed pad is connected by solder.

Therefore the permissible loss will be smaller than the specified loss by using any other board (such as 2-layer board) or the exposed pad is unconnected.

The recommended maximum load current for the DC-DC converter consisting of this IC is about 1.5A.

This load current depend on the input voltage and operating ambient temperature.

(3) Restriction of external discrete components and recommended operating conditions

To achieve a stable operation of the IC, the value of external discrete components and the voltage and the current applied to each pin should be within the recommended operating conditions.

This IC incorporates a P-channel MOSFET between the OUT pin and the VCC pin. Since the P-channel MOSFET has a parasitic diode, so if the voltage of OUT pin becomes higher than the VCC pin voltage, the current flows from the OUT pin to the VCC pin.

(4) Preventing the application of negative voltage

If rather large negative voltage is applied to any pins of this IC, internal parasitic elements start operating, and they may cause malfunctions.

Therefore the negative voltage which is applied to each terminal of the ICs must be kept above -0.3V.

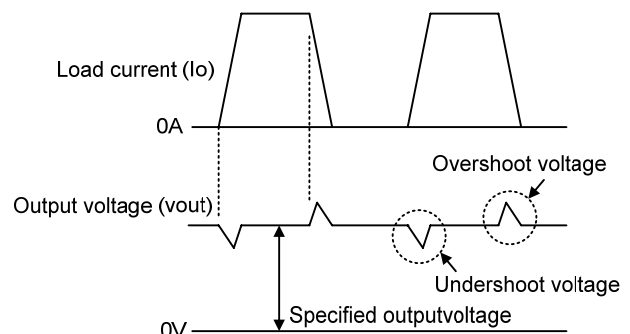
(5) Improving the transient response characteristic

The transient response characteristic of a DC-DC converter generally shows the overshoot in the output voltage when the power supply voltage is started, and the overshoot/undershoot in the output voltage when the load current changes abruptly (Fig. 7).

This IC has few overshoot at startup due to the soft start function. However, the overshoot/undershoot may occur when the load changes abruptly, depending on the conditions.

This overshoot/undershoot can be reduced by connecting a capacitor to the output voltage detection resistor as shown in Fig. 2.

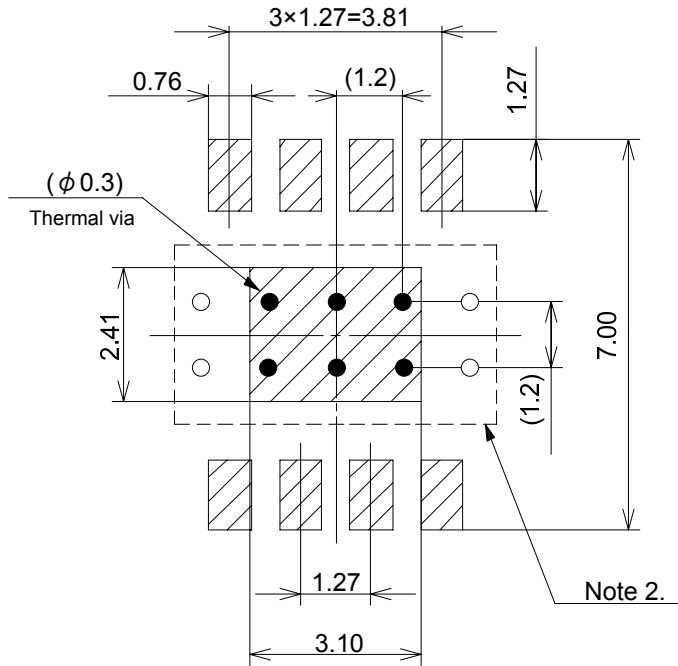
No universal constant can be proposed because it varies with the conditions. However, we believe that an appropriate effect can be produced when the constant is between hundreds of pico-Farads and tens of nano-Farads.



(6) Mounting SOP-8 (E-Pad)

Mounting the SOP-8 (E-Pad) package of this IC is by providing a 4-layer board on which to mount components for reducing the thermal resistance of the package, along with a GND pattern in the intermediate layer of the board, and connect the package E-Pad by using several thermal via.

Fig. 8 shows a recommended foot pattern.



Notes:

1. The exposed pad pattern conforms to JEDEC JESD51-5.
2. The resist is the same as that of the exposed pad. Thermal via should also be placed in positions outside of the resist opening area.

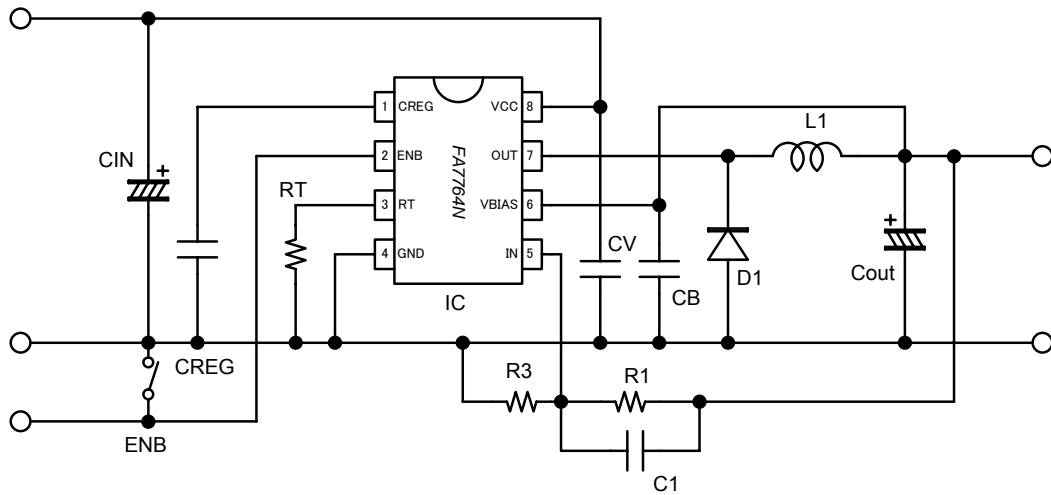
(7) Recommendation of continuous mode operation

There is a possibility of jumping up the output voltage in a discontinuous mode.

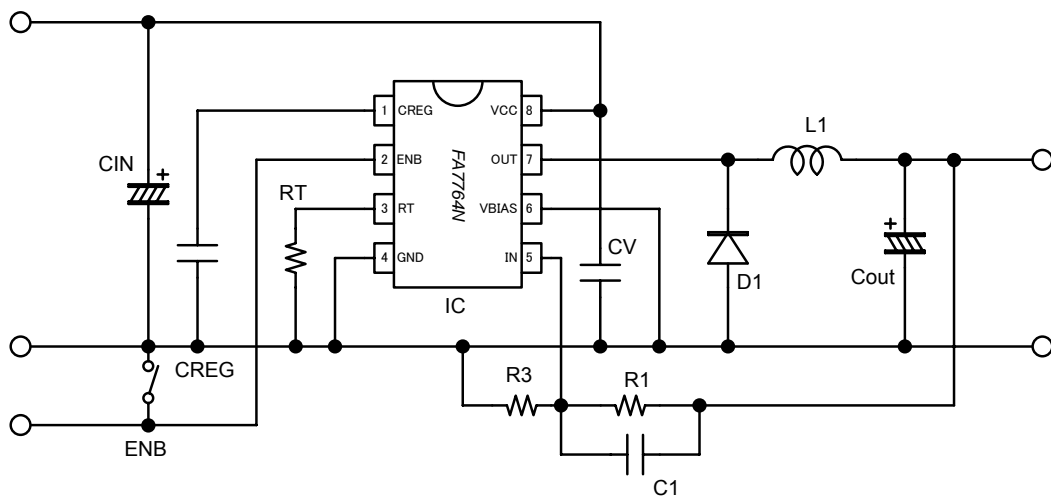
In order to prevent from this jumping up voltage, the continuous mode operation is recommended.

10. Example of applied circuits

(1) Output voltage is between 3.1V and 5.5V.



(2) Output voltage is less than 3.1V or more than 5.5V.



When you determine values and external discrete components, examine under the actual circuit condition.

Example of Parts list

Parts reference numbers are shown in the figures of applied circuits.

(1) Input voltage : 20~30V, Output voltage : 5V

Ref.	Description	Type name	Maker
IC	IC	FA7738N	Fuji
D1	Schottky Diode	SD833-06	Fuji
L1	Inductor	CDRH104R-47uH	SUMIDA
CIN	Electrolytic Capacitor	220uF/35V	Panasonic
Cout	Electrolytic Capacitor	220uF/6.3V	Panasonic
CREG	Ceramic Capacitor	0.1uF	

Ref.	Description	Type name	Maker
CV	Ceramic Capacitor	0.1uF	
CB	Ceramic Capacitor	0.1uF	
C1	Ceramic Capacitor	220pF	
RT	Resistor	22kΩ(fosc=200kHz)	
R1	Resistor	40kΩ	
R3	Rsisitor	10kΩ	

(2) Input voltage : 20~30V, Output voltage : 3.3V

Ref.	Description	Type name	Maker
IC	IC	FA7738N	Fuji
D1	Schottky Diode	SD833-06	Fuji
L1	Inductor	CDRH104R-47uH	SUMIDA
CIN	Electrolytic	220uF/35V	Panasonic
Cout	Electrolytic	220uF/6.3V	Panasonic
CREG	Ceramic	0.1uF	

Ref.	Description	Type name	Maker
CV	Ceramic	0.1uF	
CB	Ceramic	0.1uF	
C1	Ceramic	220pF	
RT	Resistor	22kΩ(fosc=200kHz)	
R1	Resistor	23kΩ	
R3	Resistor	10kΩ	