High and Low side driver IC

FA5751N /52N

Application Note

1481
1551

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Caution)

- The contents of this note will subject to change without notice due to improvement.
- The application examples or the components constants in this note are shown to help your design, and variation of components and service conditions are not taken into account. In using these components, a design with due consideration for these conditions shall be conducted.

1. Description

The FA5751N/52N is a high and low side driver IC, can drive Power MOSFETs and IGBTs that operate up to 600V. It composes elements of withstand voltage 5V/24V/600V in the same chip. Accordingly, it has a built-in High and Low side control/protection circuits, a level shift circuit of withstand voltage 600V and a driver of withstand voltage 24V.
When an HVIC is used, a high side power device can be directly driven from a microcomputer or similar, optocoupler and pulse transformer become unnecessary and high-speed response is enabled. Therefore, downsizing and high reliability of the system can be secured.

2. Features

- High side floating absolute voltage up to 600V
- High and Low side driver with 2 inputs and 2 outputs
- 3.3V logic compatible
- Turn-on and Turn-off propagation delay time typical 125ns (FA5751N), 130ns (FA5752N)
- Matched propagation delay below 30ns
- Undervoltage lockout for both channels
- Allowable offset supply voltage transient dVs/dt up to 50kV/us

List of types by function

Type	High side power supply voltage to ground VB	Control power supply voltage VBS, VCC	Output current IHO, ILO	Package
FA5650N	830V	30V	-1.4A / 1.8A	SOP-8
FA5651N	830V	30V	-1.4A / 1.8A	SOP-16
FA5751N	624V	24V	-0.20A / 0.35A	SOP-8
FA5752N	624V	24V	High side: -0.62A / 1.00A Low side: -0.56A / 0.91A	SOP-8

3. Typical Connection

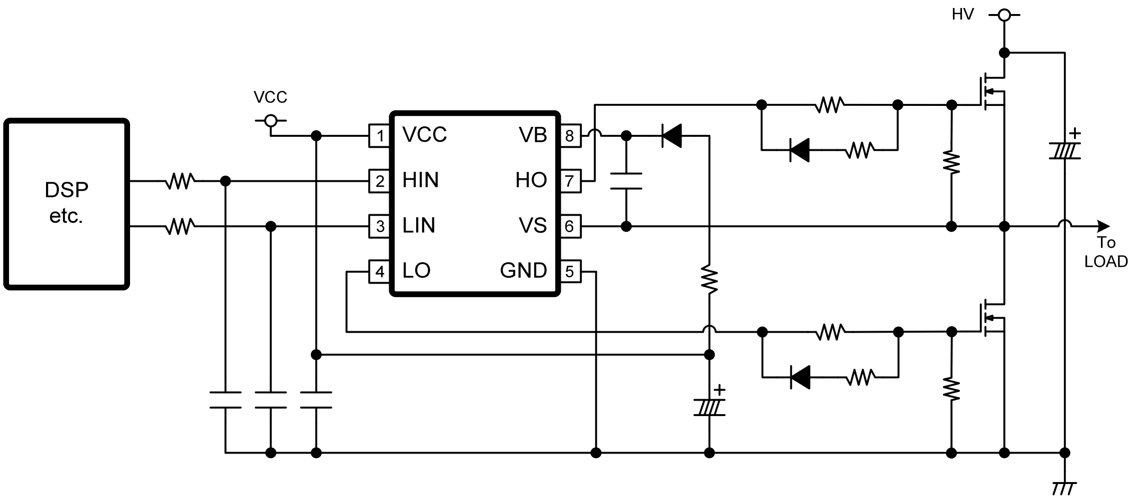
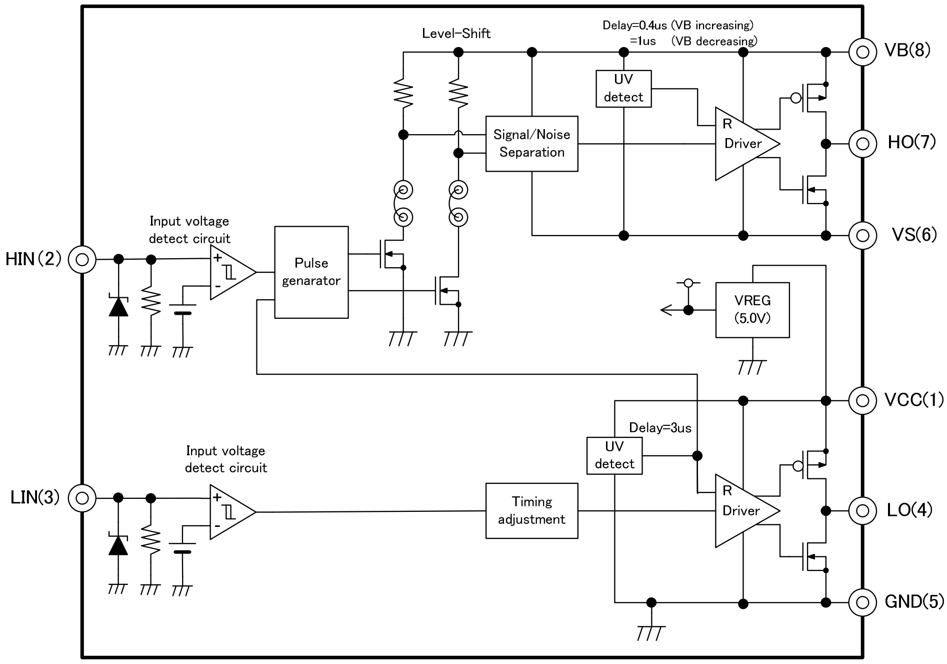


Figure 1. Typical Connection

4. Block Diagram



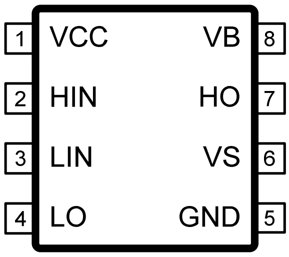


Figure 2. Block Diagram

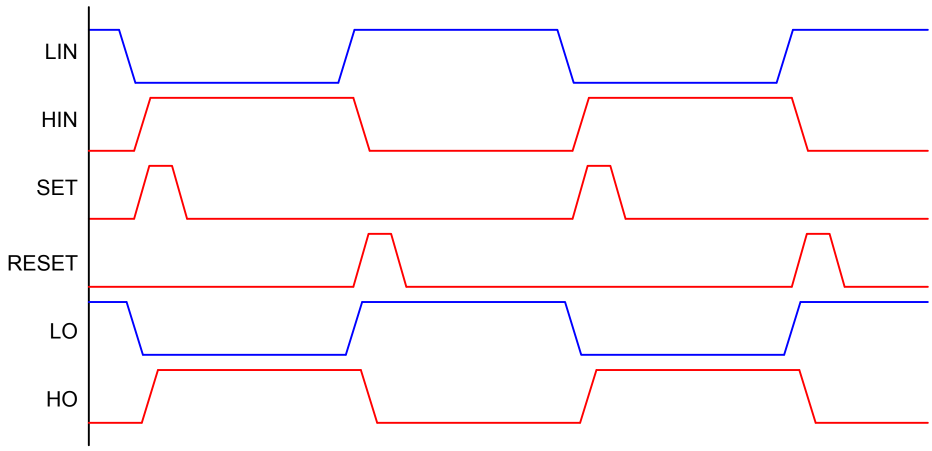
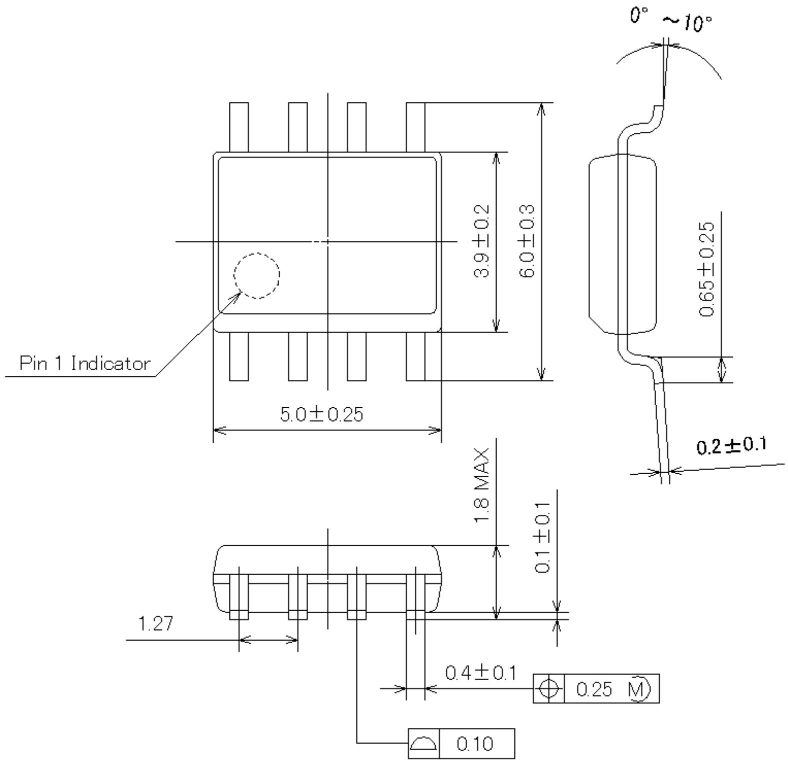


Figure 3. HVIC operation timing chart

HVIC internal blocks are shown in Figure 2. HVIC is composed of input voltage detect circuits, level shift circuits, S/N separation circuit, UV detect circuits as well as high side and low side drive circuits.

HVIC operation timing chart is shown in Figure 3. High side input signal HIN is input to the “pulse generator” block and is converted to SET and RESET one-shot pulses based on rise/fall edges. These one-shot pulses are shifted the level by the level shift circuit, and are transmitted to a high side floating circuit. The transmitted signal is shaped by elimination of common mode noise in the "signal/noise separation" block, and is produced by the high side drive circuit as a high side output signal HO. On the other hand, low-side input signal LIN is fed to the low side drive circuit through the "timing adjustment" block, and is produced as a low-side output signal LO.

5. Outline dimension



Unit: mm

Figure 4. Outline dimension SOP-8

Note: High voltage is impressed between pin 5 GND pin and pin 6 VS pin. As the minimum value of the space distance is 0.77 mm, there are cases where sufficient insulation distance cannot be secured depending on the use. In such a case, it is requested to take measures to apply coating of self-extinguishing adhesive, for instance, between terminals.

6. Pin Definitions

Pin	Symbol	Description
1	VCC	Low-side supply (connect capacitor between VCC and GND)
2	HIN	Control input for high-side gate driver output
3	LIN	Control input for low-side gate driver output
4	LO	Low-side gate driver output
5	GND	Low-side supply return
6	VS	High-side floating supply return
7	HO	High-side gate driver output
8	VB	High-side floating supply (connect capacitor between VB and VS)

7. Ratings and Characteristics

In defining a current, “+” represents a sink current and “-“ a source current.

Absolute Maximum Ratings

Stress exceeding absolute maximum ratings may malfunction or damage the device.
Never exceed power dissipation Pd.

Item	Symbol	Ratings		Units
High-side floating absolute voltage	VB	-0.3 ~ 624		V
High-side floating absolute current (no switching)	IB	0.05		mA
High-side floating supply offset voltage	VS	VB-24 ~ VB+0.3		V
High-side floating supply offset current (no switching)	IS	0.05		mA
High-side floating supply voltage (VBS=VB-VS)	VBS	-0.3 ~ 24		V
High-side floating supply current (no switching)	IBS	1.5		mA
High-side floating output voltage	VHO	VS -0.3 ~ VB+0.3		V
High-side floating output current （Ta=25℃,VB-VS=24V, PW<1us, 1pulse） *1	IHO	FA5751N	-0.20 / 0.35	A
		FA5752N	-0.62 / 1.00	A
Low-side supply voltage	VCC	-0.3 ~ 24		V
Low-side supply current (no switching)	ICC	1.5		mA
Low-side output voltage	VLO	-0.3 ~ VCC+0.3		V
Low-side output current （Ta=25℃,VCC-GND=24V, PW<1us, 1pulse） *1	ILO	FA5751N	-0.20 / 0.35	A
		FA5752N	-0.56 / 0.91	A
High-side control input voltage	VHIN	-0.3 ~ 24		V
High-side control input current	IHIN	±2		mA
Low-side control input voltage	VLIN	-0.3 ~ 24		V
Low-side control input current	ILIN	±2		mA
Allowable offset supply voltage transient	dV_S/dt	±50		kV/us
Maximum input frequency（Within Maximum dissipation）	Fmax	500		kHz
Package power dissipation (Ta=25℃)	Pd	650		mW
Package thermal resistance, junction to ambient *2	RthJA	192		℃/W
Operating ambient temperature	Ta	-50 to +125		℃
Junction temperature	Tj	-50 to +150		℃
Storage temperature	Tstg	-50 to +150		℃

*1: Peak current at LO/HO pin may flow to rated value neither according to VCC/VBS voltage nor temperature conditions. Please consider power supply voltage and load current well and use this IC within maximum power dissipation, operating junction temperature and recommended ambient temperature in operation. The IC may cross over maximum power dissipation at normal operating condition by power supply voltage or load current within peak current absolute maximum rating value.

*2: JEDEC STANDARD Test board

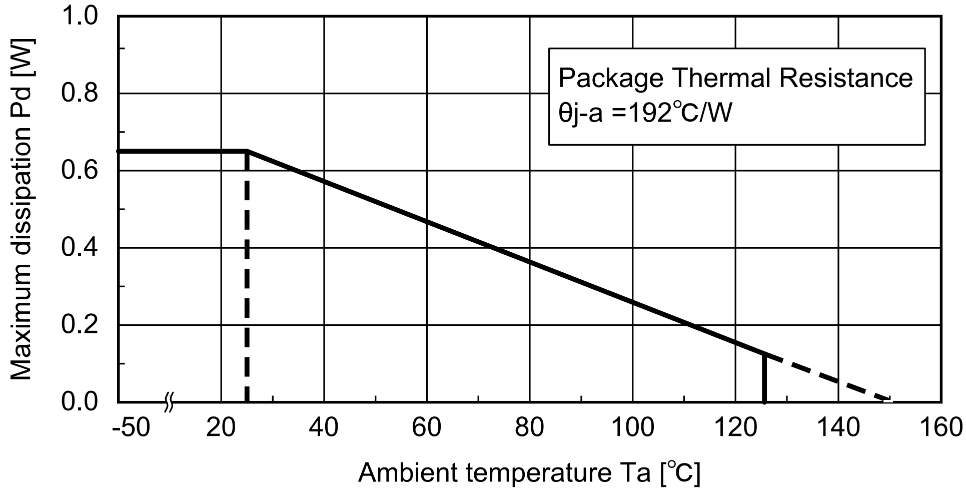


Figure5. Maximum Dissipation Curve

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Units
High-side floating absolute voltage	VB	VS+12	VS+15	VS+18	V
High-side floating supply offset voltage *1	VS	-5	-	480	V
High-side floating supply voltage (VBS=VB-VS)	VBS	12	15	18	V
High-side floating output voltage	VHO	VS	-	VB	V
Low-side supply voltage	VCC	12	15	18	V
Through rate of raising low-side supply voltage	dVcc/dt	20	-	-	V/us
Low-side output voltage	VLO	0	-	VCC	V
High-side control input voltage	VHIN	0	5	VCC	V
Low-side control input voltage	VLIN	0	5	VCC	V
High-side control input frequency	FHIN	-	-	200	kHz
Low-side control input frequency	FLIN	-	-	200	kHz
Operating ambient temperature	Ta	-50	-	125	℃

*1: The voltage of the VB pin is over 10V.

DC Electrical Characteristics

Tj=25℃, VCC=15V, VS=GND, VB=15V, HO=open, LO=open, unless otherwise specified.
The voltage described in the condition is DC input and is not AC input.
Note) "-": These items are not guaranteed.

(1) Input (HIN pin, LIN pin)

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Logic "1" input voltage	VIH	VHIN or VLIN increasing DC input voltage at output voltage high.	1.7	2.1	2.5	V
Logic "0" input voltage	VIL	VHIN or VLIN decreasing DC input voltage at output voltage low.	1.0	1.3	1.6	V
Logic "1" input bias current	IIN+	VHIN or VLIN=5V	0.06	0.15	0.36	mA
Logic "0" input bias current	IIN-	VHIN or VLIN=0V	-	0	5.0	uA
Minimum on pulse width *2	twon	VHIN or VLIN=0V→5V→0V dV/dt=5kV/us	5	30	100	ns
Minimum off pulse width *3	twoff	VHIN or VLIN=5V→0V→5V dV/dt=5kV/us	5	30	100	ns

*2: IC holds off-state if input on pulse width is smaller than minimum on pulse width.
*3: IC holds on-state if input off pulse width is smaller than minimum off pulse width.

Relations of input signal and output signal is shown in a figure 6. When pulse width of an input signal is less than minimum on pulse width twon or minimum off pulse width twoff, input signal is not transmitted to the output terminal.

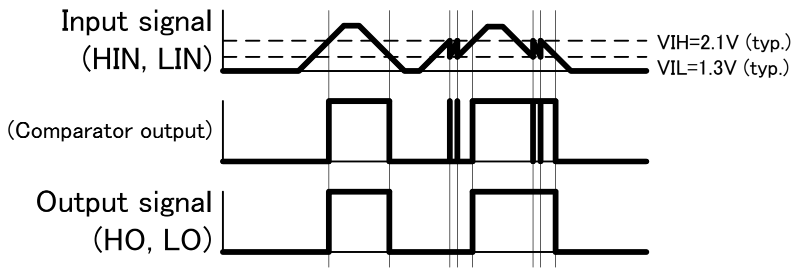


Figure 6. Minimum on/off Pulse Width

(2)Driver Output (HO pin, LO pin)

Item	Symbol	Conditions		Min.	Typ.	Max.	Units
High level output voltage	VOH	VHIN or VLIN=5V Io=-10mA		14.0	14.7	-	V
Low level output voltage	VOL	VHIN or VLIN=0V Io=10mA		-	0.12	0.36	V
HO output high short circuit pulse current *4	IOH_HO	Vo=0V, PW<1us,1pulse	FA5751N	-300	-200	-120	mA
			FA5752N	-620	-410	-250	mA
HO output low short circuit pulse current *4	IOL_HO	Vo=15V, PW<1us,1pulse	FA5751N	250	350	550	mA
			FA5752N	470	660	1030	mA
LO output high short circuit pulse current *4	IOH_LO	Vo=0V, PW<1us,1pulse	FA5751N	-300	-200	-120	mA
			FA5752N	-560	-370	-220	mA
LO output low short circuit pulse current *4	IOL_LO	Vo=15V, PW<1us,1pulse	FA5751N	250	350	550	mA
			FA5752N	420	580	910	mA
Turn-on propagation delay	ton	VHIN or VLIN=0V to 5V dV/dt=5kV/us FHIN or FLIN=100kHz Duty=50%	FA5751N	80	125	170	ns
			FA5752N	85	130	175	ns
Turn-off propagation delay	toff	VHIN or VLIN=5V to 0V dV/dt=5kV/us FHIN or FLIN=100kHz Duty=50%	FA5751N	80	125	170	ns
			FA5752N	85	130	175	ns
Delay matching, high-side and low-side turn on/off *5	MT	VHIN, VLIN=0V to 5V VHIN, VLIN=5V to 0V dV/dt=5kV/us		-30	0	30	ns
Turn-on rise time	tr	CL=1000pF	FA5751N	30	135	340	ns
			FA5752N	20	75	130	ns
Turn off fall time	tf	CL=1000pF	FA5751N	30	135	340	ns
			FA5752N	20	75	130	ns

*4: Guaranteed by design.
*5: MT = ton(HS) – ton(LS), toff(HS) – toff(LS)

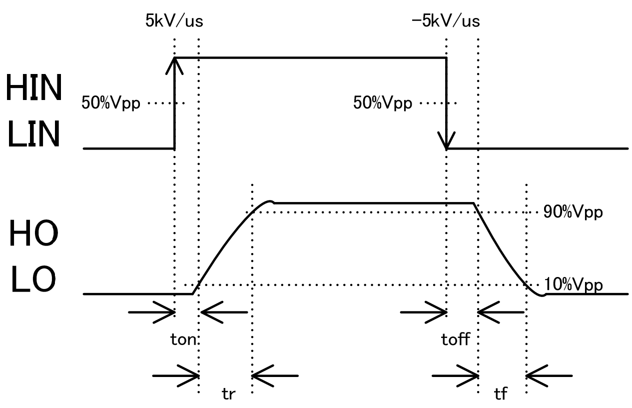


Figure 7. Switching Time Waveform Definitions

(3)Under Voltage Lockout (VCC pin, VB pin)

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
VCC and VBS supply under-voltage positive going threshold voltage *6,7	VBSON VCCON	VB or VCC increasing DC input voltage	8.0	8.9	9.8	V
VCC and VBS supply under-voltage negative going threshold voltage *6	VBSOFF VCCOFF	VB or VCC decreasing DC input voltage	7.4	8.2	9.0	V
VCC and VBS supply under-voltage lockout hysteresis voltage	VBSHYS VCCHYS	VBSON-VBSOFF VCCON-VCCOFF	0.3	0.7	1.1	V
VBS supply under-voltage lockout filter time *8	tBSUV	VB increasing	0.1	0.4	1.0	us
		VB decreasing	0.1	1.0	2.0	us
VCC supply under-voltage lockout filter time *8	tCCUV		1	3	10	us
VBS supply minimum operating voltage *9	VBSMIN	IHO_sink=1mA	1.8	3.1	4.0	V
VCC supply minimum operating voltage *9	VCCMIN	ILO_sink=1mA	1.8	3.1	4.0	V

*6: Positive going threshold voltage > Negatine going threshold voltage

*7: In the case of 2.5V/us＜dVcc/dt＜10V/us, the LO pin has a possibility of outputs on-pulse.

*8: ・VBS(VCC) supply under-voltage lockout filter time: tBSUV increasing (tCCUV)

It is the time to VHO(VLO)=H , after VBS(VCC) voltage reaches the VBS(VCC) supply under-voltage positive going threshold voltage.

・VBS supply under-voltage lockout filter time: tBSUV decreasing

It is the time to VHO=L , after VBS voltage reaches the VBS supply under-voltage negative going threshold voltage.

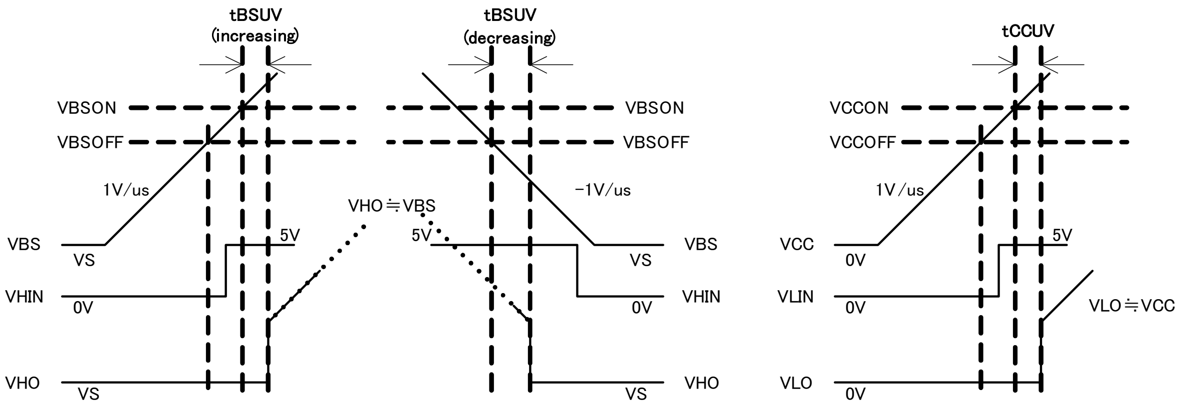


Figure 8. UVLO filter time Definitions

*9: In the case of （VB-VS）<VBSMIN or VCC<VCCMIN, the switching device may operate abnormally because the HO pin output or the LO pin output turns on regardless of the HIN input or the LIN input. Reference to “10. Design Guidelines”.

(4) Power Supply Current (VCC pin, VB pin)

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Offset supply leakage current	ILK	VB=VS=600V VHIN=VLIN=0V	-	-	1	uA
Quiescent VBS supply current	IBS	VHIN=VLIN=0V DC input voltage	20	80	160	uA
Quiescent VCC supply current	ICC	VHIN=VLIN=0V DC input voltage	230	280	430	uA
Dynamic operating supply current	IOP	VHIN=VLIN=0V⇔5V FHIN=FLIN=100kHz Duty=50% dV/dt=5kV/us	280	560	1120	uA

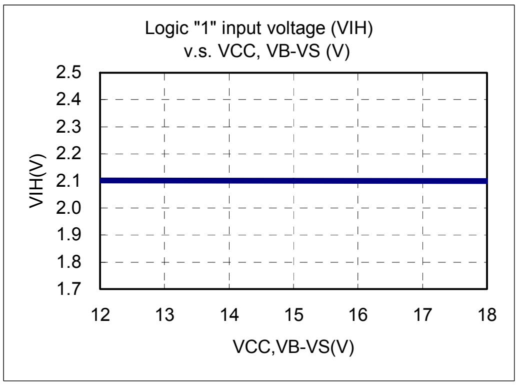
8. DC Typical Characteristics

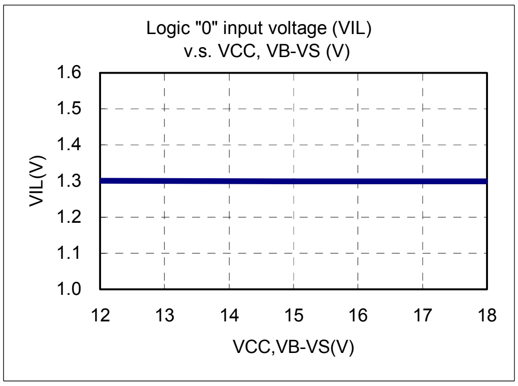
Tj=25℃, VCC=15V, VS=GND, VB=15V, HO=open, LO=open, unless otherwise specified.

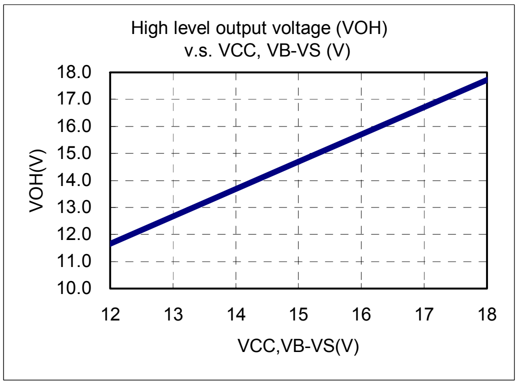
The data stated in this chapter shows the typical IC characteristics and does not guarantee the performance.

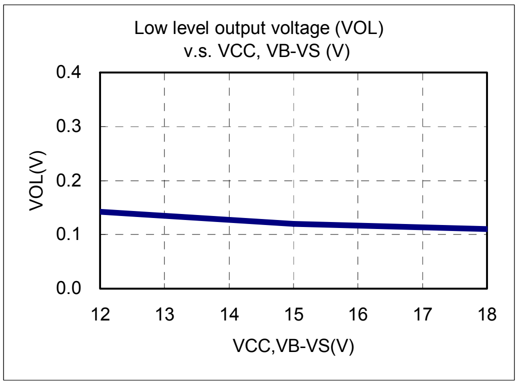
FA5751N /52N common characteristics

Voltage-dependence

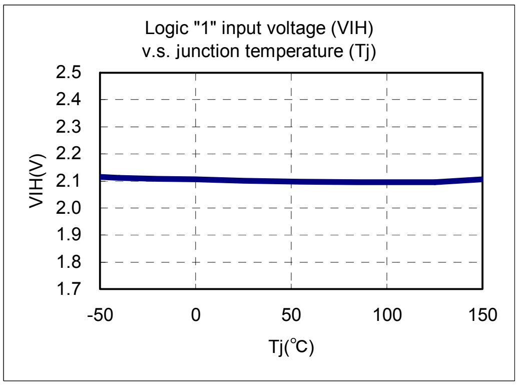


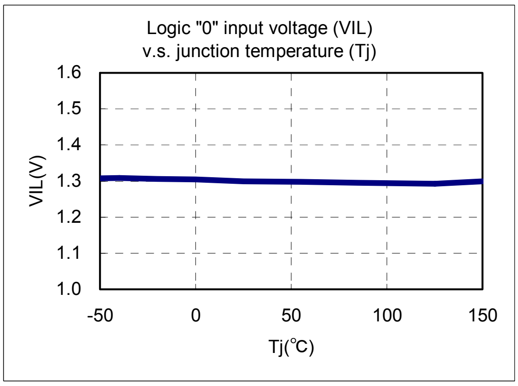


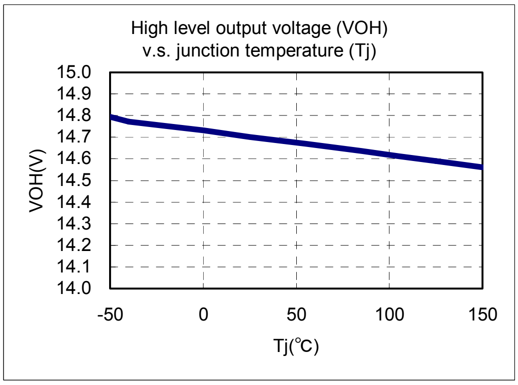


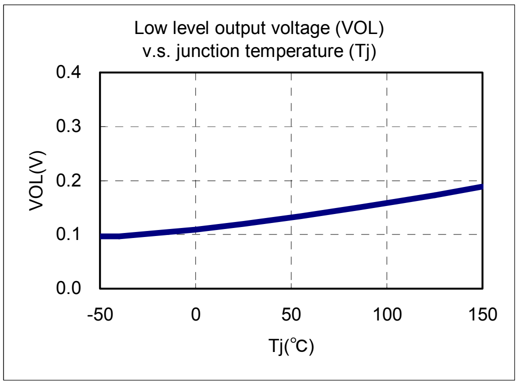


Temperature-dependence



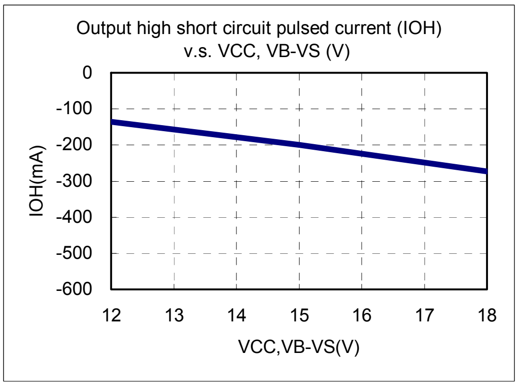


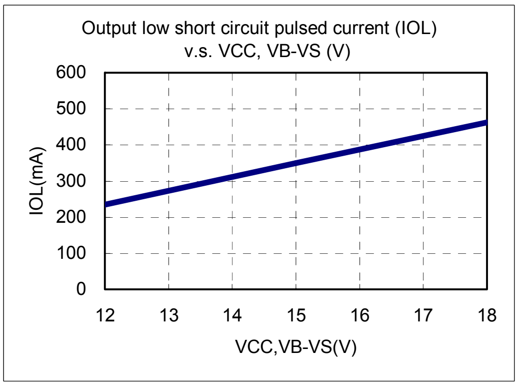


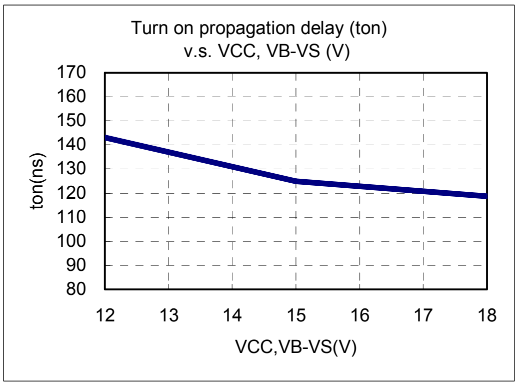


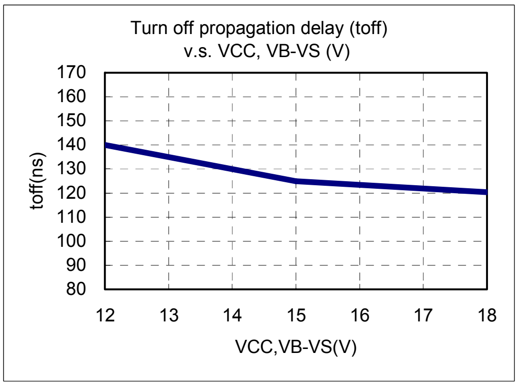
Characteristics only for FA5751N

Voltage-dependence









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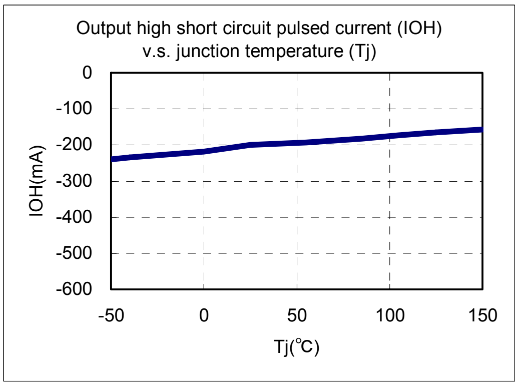
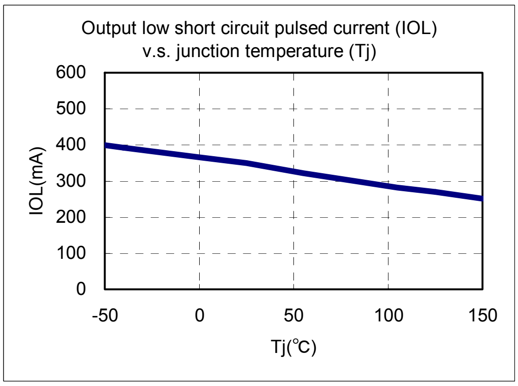
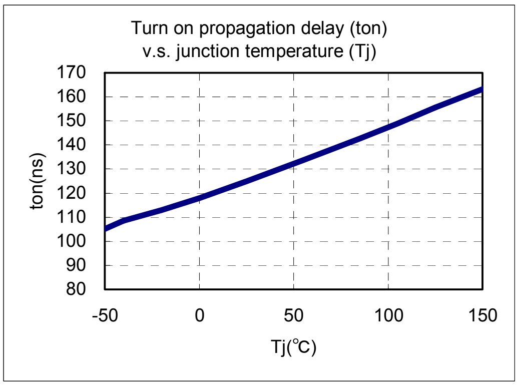
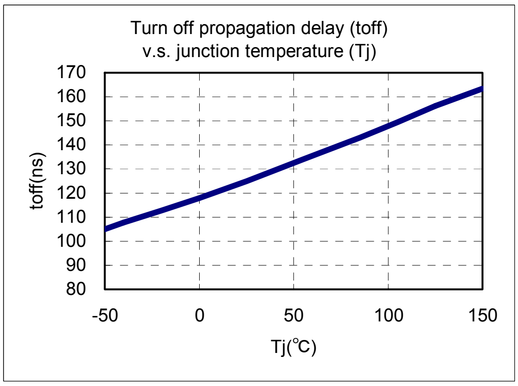


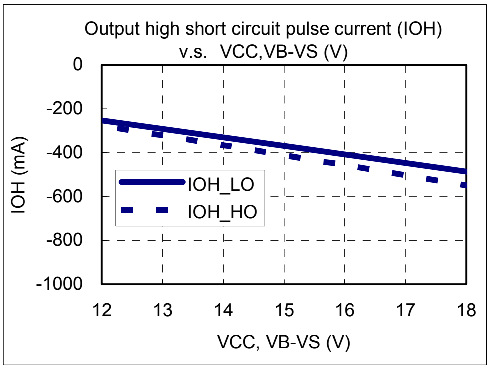


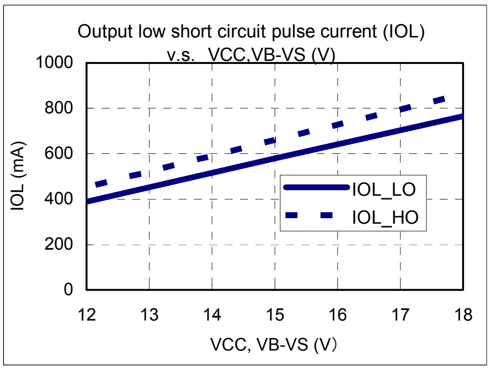


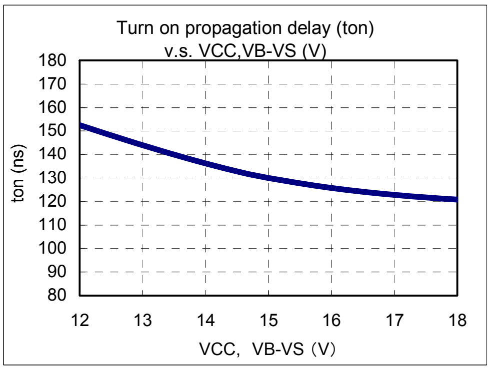


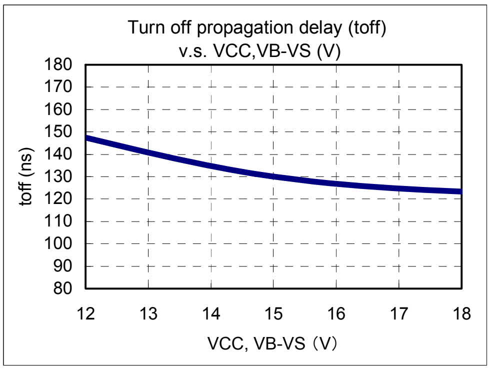
Characteristics only for FA5752N

Voltage-dependence

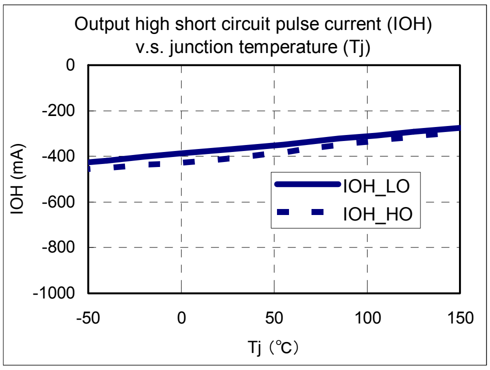


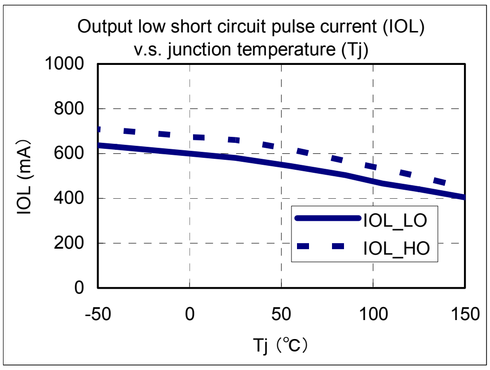


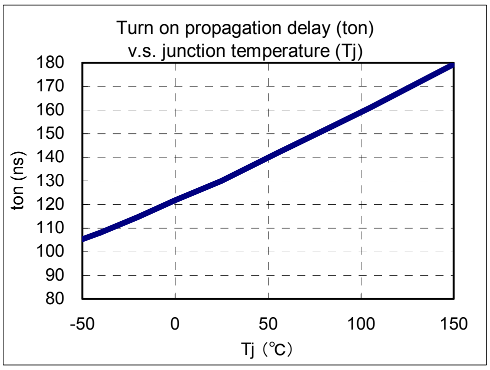


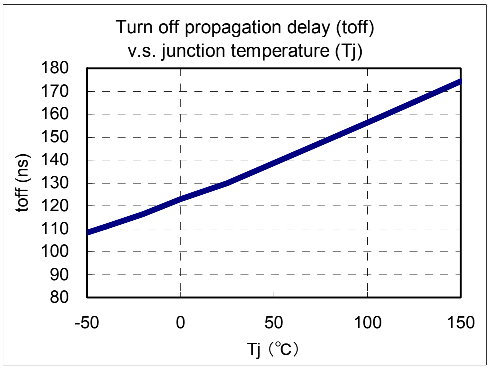


Temperature-dependence



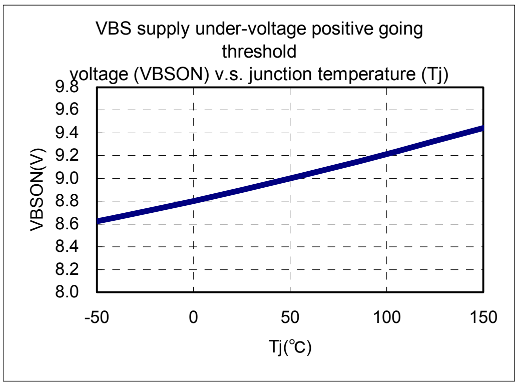


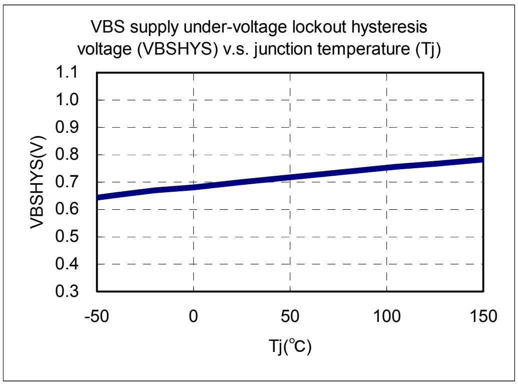


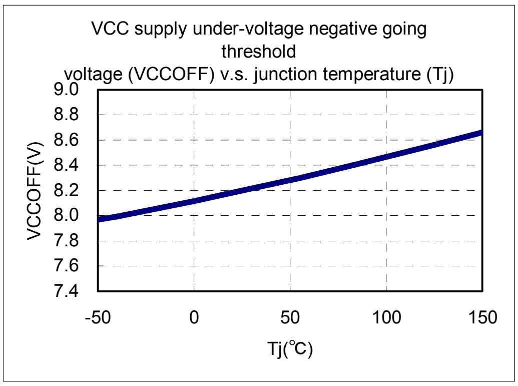


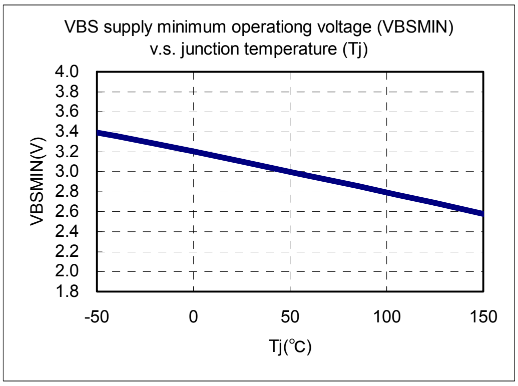
FA5751N /52N common characteristics

Temperature -dependence

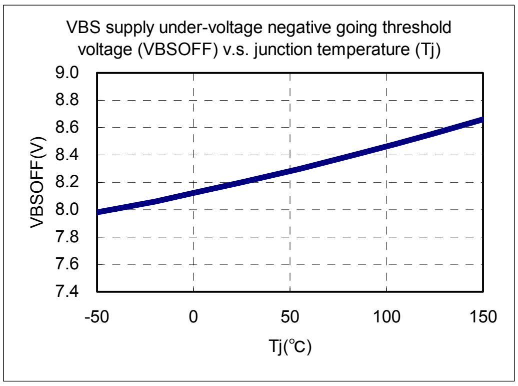


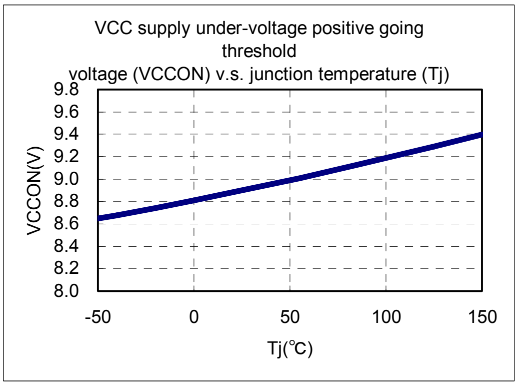


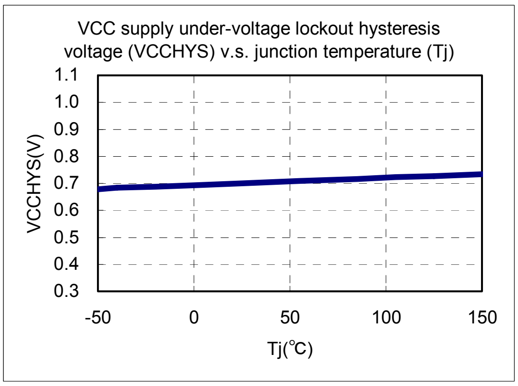


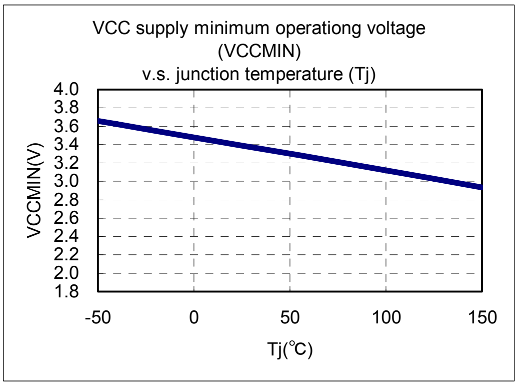


Temperature-dependence





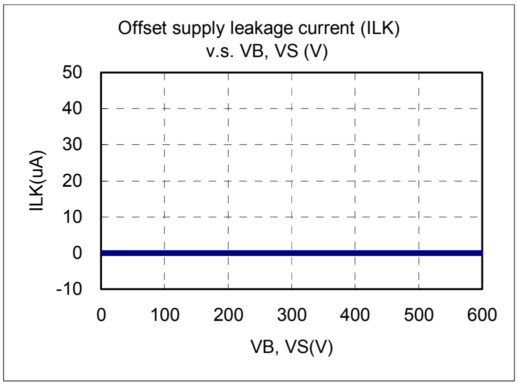


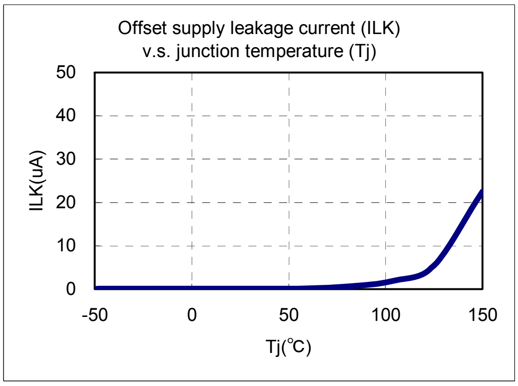


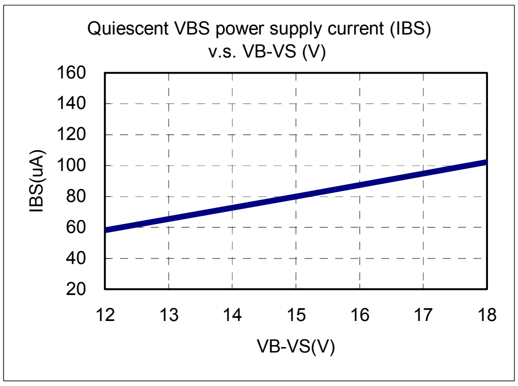
FA5751N /52N common characteristics

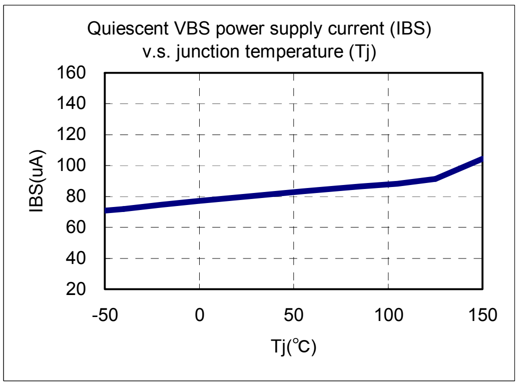
Voltage-dependence

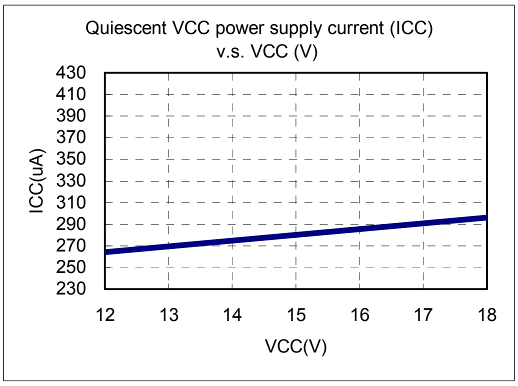
Temperature-dependence

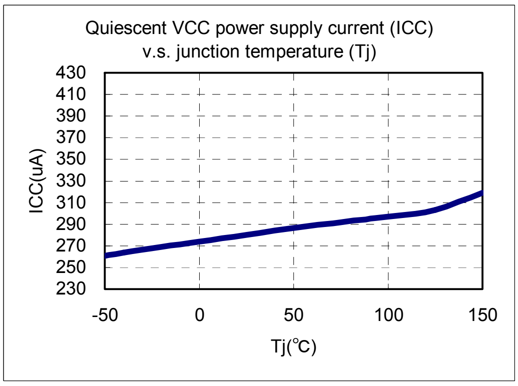


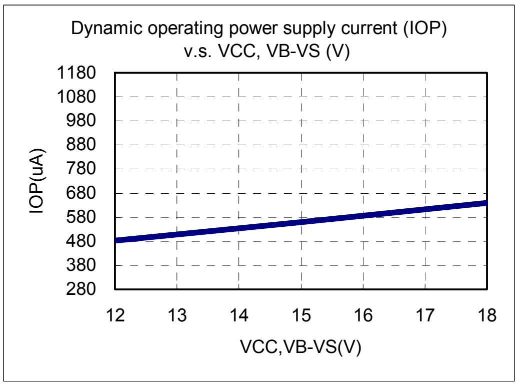


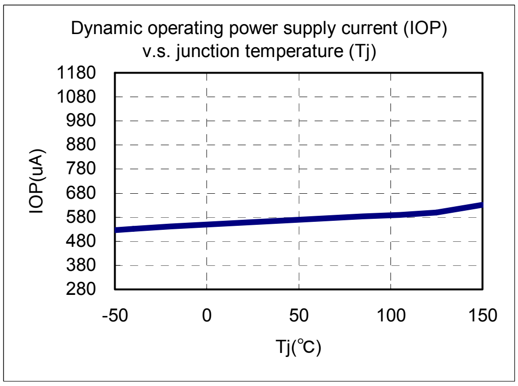












9. Start/stop operation

Low-side operation is shown in Figure 9. At startup, the LO output is indeterminate while the VCC voltage is lower than minimum operating voltage VCCMIN. The LO output is produced after the VCC voltage exceeds the ON threshold voltage VCCON.

At shutdown, the LO output stops when the VCC voltage drops lower than the OFF threshold voltage VCCOFF. When the VCC voltage further drops lower than the VCCMIN, the LO output becomes indeterminate. The LO operation is not dependent on high side power supply voltage VBS.

The high side operation is shown next. Figure 10 shows the case where VCC rises and falls under the condition of established VBS. When the VCC voltage exceeds the ON threshold voltage VCCON and HIN is applied, the HO output is produced. When the VCC voltage drops lower than the OFF threshold voltage VCCOFF, the HO output is stopped. In this case, there is no state where the HO logic becomes indeterminate.

Figure 11 shows the case where VBS rises and falls under the condition of established VCC. When the VBS voltage exceeds the ON threshold voltage VBSON and HIN is applied, the HO output is produced. When the VBS voltage drops lower than the OFF threshold voltage VBSOFF, the HO output is stopped. The HO output is indeterminate when the VBS voltage is lower than the threshold voltage VBSMIN.

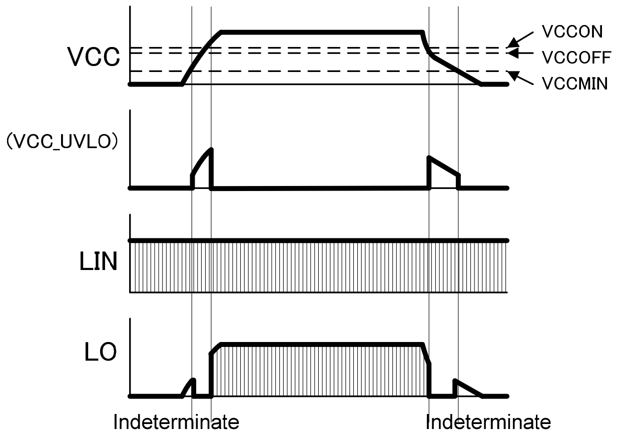


Figure 9. Low-side operation of VCC rising/falling

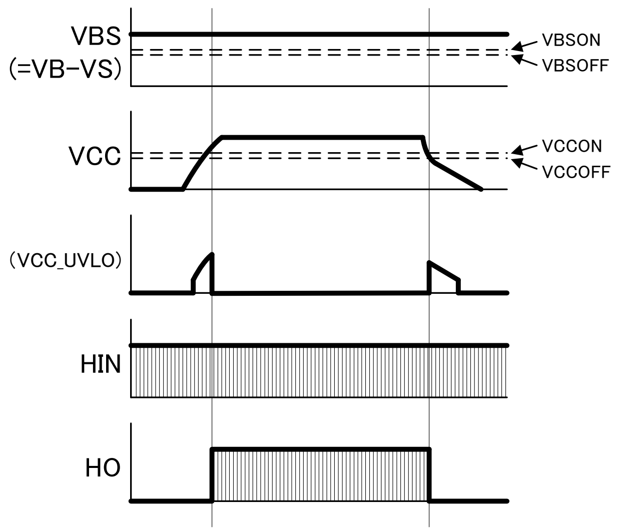


Figure 10. High-side operation of VCC rising/falling when VBS is established

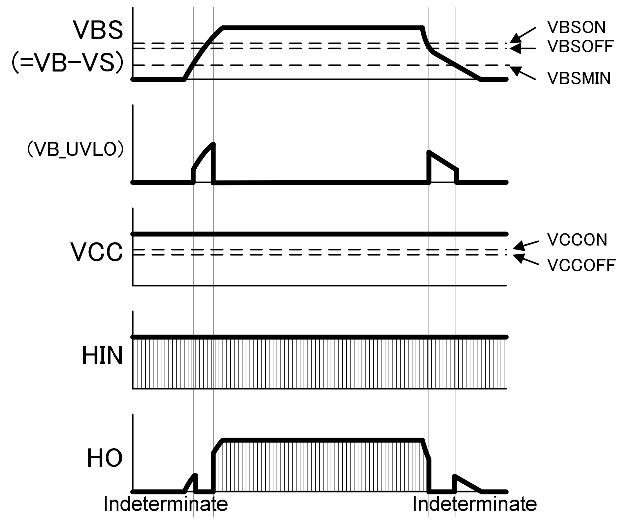


Figure 11. High-side operation of VBS rising/falling when VCC is established

10. Design Guidelines

10.1 Prevention of high-side MOSFET self-turn-ON

In the case where VBS or VCC is lower than the minimum operating voltage, the output signal (HO, LO) may appear without regard to the input signal (HIN, LIN). Especially in the case where VBS is lower than the minimum operating voltage VBSMIN, since the HO voltage is undefined, turning on of the low-side MOSFET might cause a self turning on of the high-side MOSFET by the ratio between the reverse transfer capacitance Crss and the input capacitance Ciss of the high-side MOSFET. In such a case, set an appropriate capacitor Cadd between the gate and the source of the high-side MOSFET for avoiding the rise of the gate voltage, or do not use a MOSFET of low threshold voltage VGS (th).
Select the appropriate capacitance Cadd referring to the following formula. As a high voltage power MOSFET has a characteristic of rapid decreasing Crss after Vds exceeds around 10V and the influence of Crss for the gate voltage becomes smaller, put the amount of Vds changing as ΔVds from 0V to the value near the selected Crss. And as VGS (th) has a characteristic becoming lower at the higher temperature, select the capacitance Cadd having enough margin by considering a higher temperature condition.

$$VGS(th) > \frac{Crss}{Ciss - Crss + Cadd} \times \Delta Vds$$

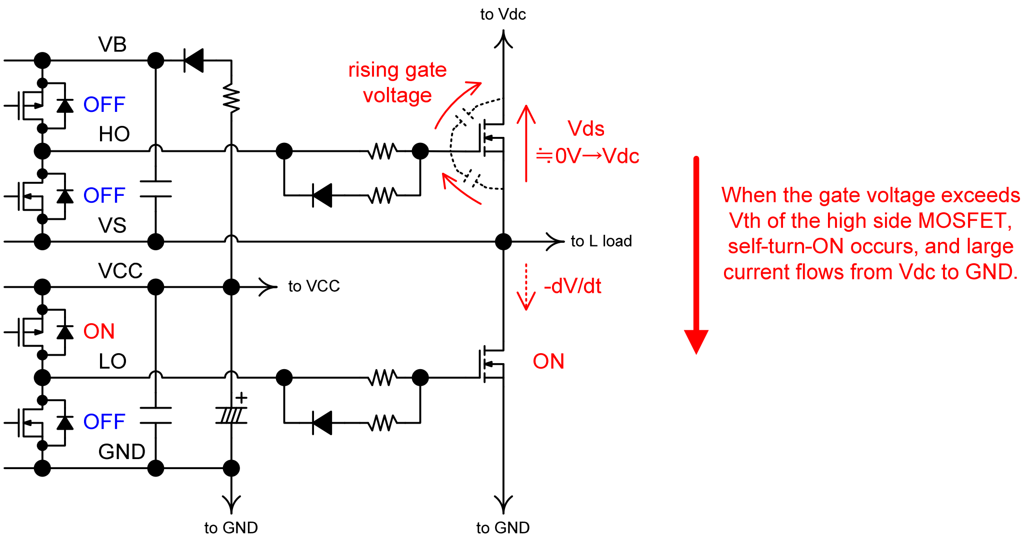


Figure 12. Lifting of high-side FET’s gate voltage when the Low-side FET turns on

10.2 Application circuit which use FWD positively

In applications such as motor control we have positive switching operations of a built-in diode of MOSFET, or of a freewheel diode FWD which is a reverse parallel connection to IGBT. In the case of IGBT, when the high side IGBT turns on while current is flowing through FWD of the low side IGBT, reverse-recovery-current into the FWD will make a steep dV/dt. And the rapidly rising of the voltage between the collector and the emitter by this steep dV/dt will raise the gate voltage by the current flowing through the capacitance between the gate and the collector. As the result, you will see the problem of increasing the turn-on loss of IGBT. Take the following measures to avoid this problem.

- Reduce dV/dt by slowing the turning-on speed.
- Reduce the impedance between gate and emitter by reducing the turning-off resistance.
- Reduce the wiring impedance by minimizing the wiring distance between HVIC and IGBT.
- Add a gate-reverse-biasing circuit.

Since this HVIC has no built-in reverse-biasing circuits, it is necessary to mount buffer circuits with a built-in reverse-biasing circuit between the HVIC and the power devices, in the case that power devices are used in reverse-biased at turning-off.

10.3 Impressing of negative voltage to high-side VS pin

When Q1 of the high-side MOSFET is turned off from on-state while Q2 of the low-side MOSFET is off, the current which was flowing through Q1 circulates through the body diode of Q2 and the load. At this moment, by the inductance and the current changing rate, the VS terminal voltage falls tens of volts from the ground potential voltage during the period of hundreds of ns, and so IC may malfunction or break when absolute maximum rating is exceeded.

Fuji HVIC secures high negative-withstand-voltage by contriving the device layout in IC. (Negative-withstand-voltage means the voltage in which output signals do not malfunction to input signals.) The following figure shows the typical measurements of the negative-withstand-voltage against the pulse width. Fuji HVIC has negative-withstand-voltage of 3 or more times than competitor's at the time of pulse width 1us, and has the feature which may not malfunction easily. As the result, Fuji HVIC has advantage when the design does not permit the reduction of the switching speed or of the parasitic inductance of wiring patterns.

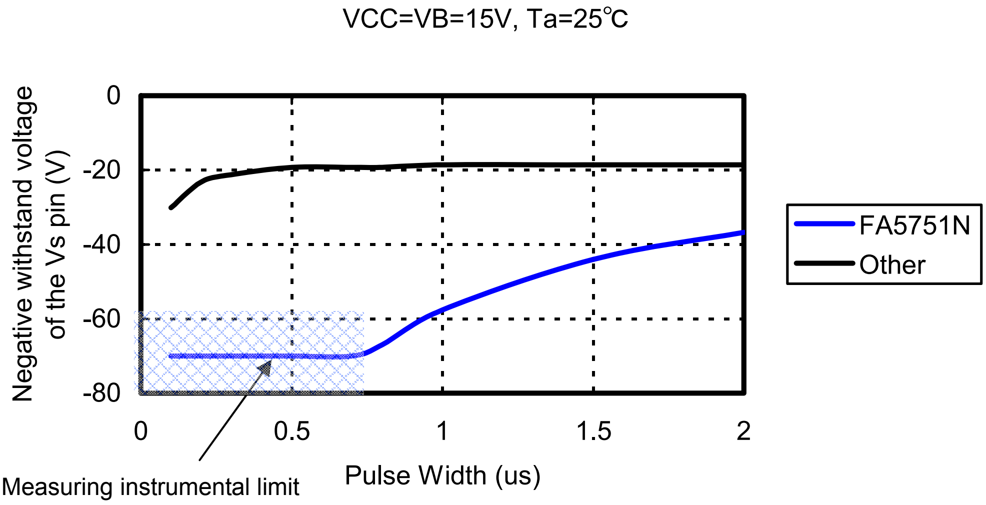


Figure 13. Comparison of negative-withstand-voltage tolerance of VS pin
(The data described here indicates typical IC characteristics, and does not guarantee characteristics.)

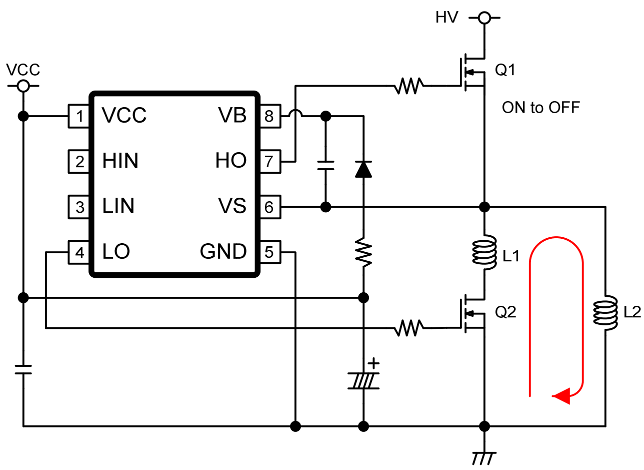


Figure 14. Impressing of negative voltage to VS pin

10.4 Bootstrap circuit for high-side gate drive power supply

Driving the high-side MOSFET Q1 requires the power supply voltage VBS based on the Q1's source potential voltage. The high side power supply voltage VBS easily consists of an external bootstrap circuit. And it has an advantage that the system cost can be lower than preparing floating power supplies for VBS.

(1) Basic Operation of Bootstrap Circuit

When the low-side MOSFET Q2 turns on, VS voltage is reduced to the ground potential and the low side power supply VCC charges the capacitor C1 through the diode D1. When Q2 turns off, VS becomes a floating potential and the charging loop is shut off. And the electric charge of C1 will drive Q1, being HIN inputted.

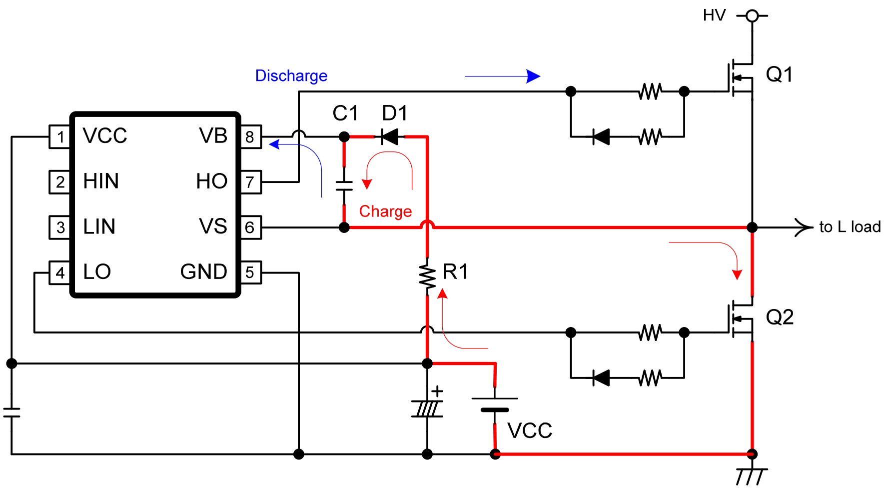


Figure 15. Basic Operation of Bootstrap Circuit

(2) Selecting the Bootstrap Capacitor C1

When Q2 is off-state and Q1 is being driven, the high side power supply voltage VBS is reduced gradually through the high side operating current IBS, the gate charging current of Q1 and the leakage current of C1 since C1 is not being charged. Therefore, it is necessary to select the capacitance of C1 so that VBS voltage may not fall to below the off-threshold-voltage VBSOFF while Q1 is being driven. The capacitance indispensable for C1 is calculated by the following formula. We recommend that the C1 value is twice or more than the calculated.

$$C1 = \frac{Qg + IBS \times Ton + Icbs(leak) \times Ton}{Vcc - VBSOFF - Vf - VLS}$$

Qg: Gate charging amount of MOSFET, IGBT (Q1)
IBS: High side operating current of IC
Ton: High side maximum on time
Icbs (leak): Leak current of bootstrap capacitor (C1)
VCC: Low side power supply voltage
VBSOFF: High side off threshold voltage
Vf: Diode forward direction voltage of bootstrap (D1)
VLS: On voltage of low side MOSFET, IGBT (Q2)

We can charge the capacitance C1 only while the low side MOSFET Q2 is on-state (and the high side MOSFET Q1 is on). And it is necessary to set the on-state period Ton2 of Q2 so that the q electrically discharged from C1 while Q2 is off can be fully recharged.

$$q = CE(1 - e^{-\frac{ton2}{CR}})$$

C: Capacitance of C1
E: Voltage impressed between the both ends of C1
CR: Time constant of the series circuit of C1 and R1

(3) Selecting the Bootstrap Diode D1

Select the fast recovery diode with a short reverse recovery time. Using a diode for D1 with a long reverse recovery time decreases the power supply efficiency of VCC (the low side power supply) since the reverse recovery current to VCC becomes large when high-side is on. And ripples to VCC might cause malfunction. Select the diode having a withstand voltage more than the low-side power device, considering of derating. For instance, to use Fuji's FMV11N60E for the low-side power device, it is necessary to select the diode for D1 having a withstand voltage exceeding 600V.
The average current IFAV can be roughly calculated by the product of the total gate-charging amount Qg and the operating frequency fsw of the power device. When Qg=73nC(max) and fsw=100kHz are assumed, IFAV can be calculated by the following.

$$IFAV = Qg \times fsw = 7.3mA$$

And the peak current can be calculated by dividing the maximum low side power supply voltage VCC by the resistance R1.

(4) Selecting the Resistor in Series with the Bootstrap Diode

Make sure to insert the resistor R1 preventing the initial rush current charging C1. And to prevent breaking the diode D1, select the resistance of R1 so that the current flowing into D1 is absolutely below the peak current acceptable of D1.

(5) Other Guidelines

- The high side power supply voltage VBS is lower than the low side power supply voltage VCC due to the on-state voltage of D1 and Q2, and, in addition, due to the on-state period of Q2. Thus, it is necessary to take notice of the difference of the gate voltages of Q1 and Q2.
- If Q1 switches and Q2 keeps off-state, the VBS voltage falls rapidly and the HO terminal might be easily suspended.
- At the startup, it is necessary to charge C1 initially by turning on Q2. And secure the on-period of Q2 so that the voltage of C1 should be set high enough to the off-threshold voltage VBSOFF.
- As is described above, there are constraints in preparing high side power supplies by bootstrap circuits. If some problems arise from using bootstrap circuits, we recommend using DC/DC converters insulated by the transformer to make stable power supplies to HVIC.
- When using IGBT as power devices, not using power MOSFET, the saturation voltage Vce (sat) between the collector and the emitter very depends upon the gate voltage. Lower gate voltage makes the saturation voltage higher, and increases the steady-state loss. Thus, set the power supply voltage to be able to secure the recommended gate voltage described in the IGBT data sheet. In general, the recommended IGBT's gate voltage is 15V, and the power MOSFET's is 10V.

10.5 Layout guidelines

Consider the points described below in the pattern layouts. Design the patterns to satisfy the safety standards in the countries or the areas where the products are used. And check the layout patterns and the circuit constants fully enough in the actual products.

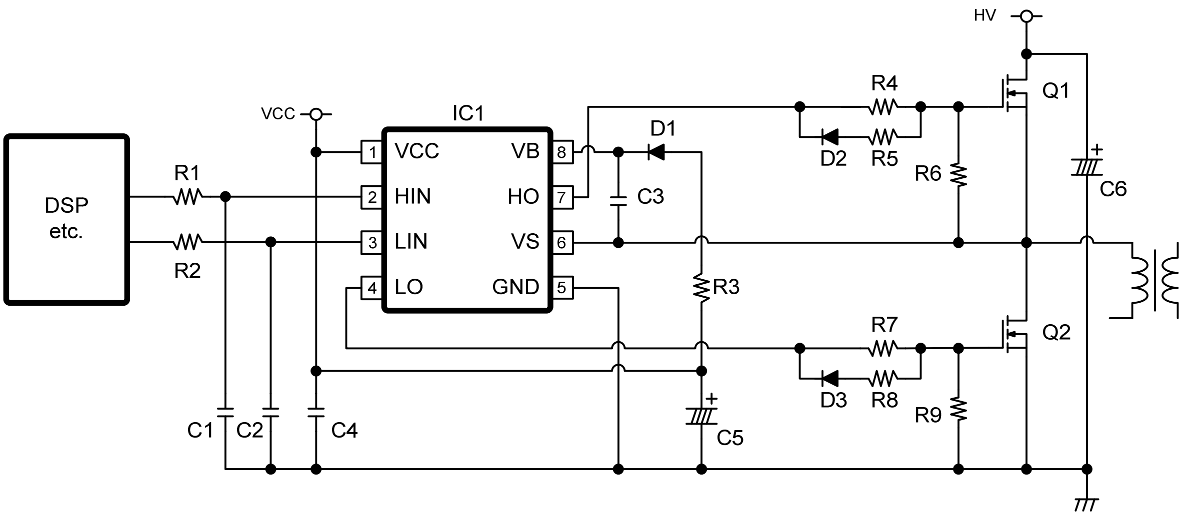


Figure 16. Typical circuit

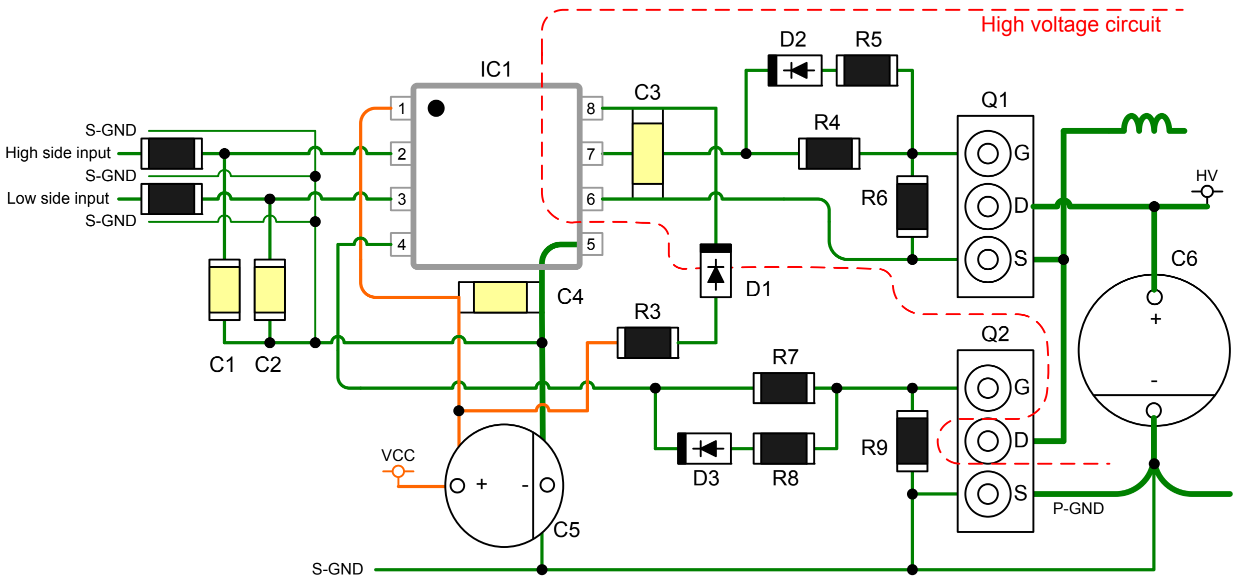


Figure 17. Typical layout

- Separate the power line P-GND in which the main current flows from the signal line S-GND in which the control current flows. If both are in common, S-GND's electric potential is fluctuated by the main current and the product may malfunction.
- If noises influence the input signals of IC, CR filters must be arranged near by the pin No.2 (HIN) and the pin No.3 (LIN).
- It is recommended to arrange the S-GND patterns adjacent to the HIN line and the LIN line, in order to avoid cross talks between HIN and LIN and to reduce interference between parallel lines on the printed circuit board.
- Arrange the HIN, LIN and S-GND patterns away from the power circuits.
- Not to receive the induction noise, minimize the loop area made by the power supply pattern driving a gate and by the gate terminal. Larger loop area might cause over-voltage destruction or malfunction of the MOSFET. And do keep the P-GND pattern from passing to this gate current loop.

- Arrange the bootstrap capacitor C3 near by the pin No.6 (VS) and the pin No.8 (VB).
- Minimize the loop area made by Q1, Q2 and C6 patterns. It is effective for suppressing the surge voltage and the radiation noise of the power devices.
- The surge voltage generated between VS and GND can be suppressed by reducing the pattern inductance of VS, Q1 source, Q2 drain, Q2 source and GND pin.

11. Truth Table

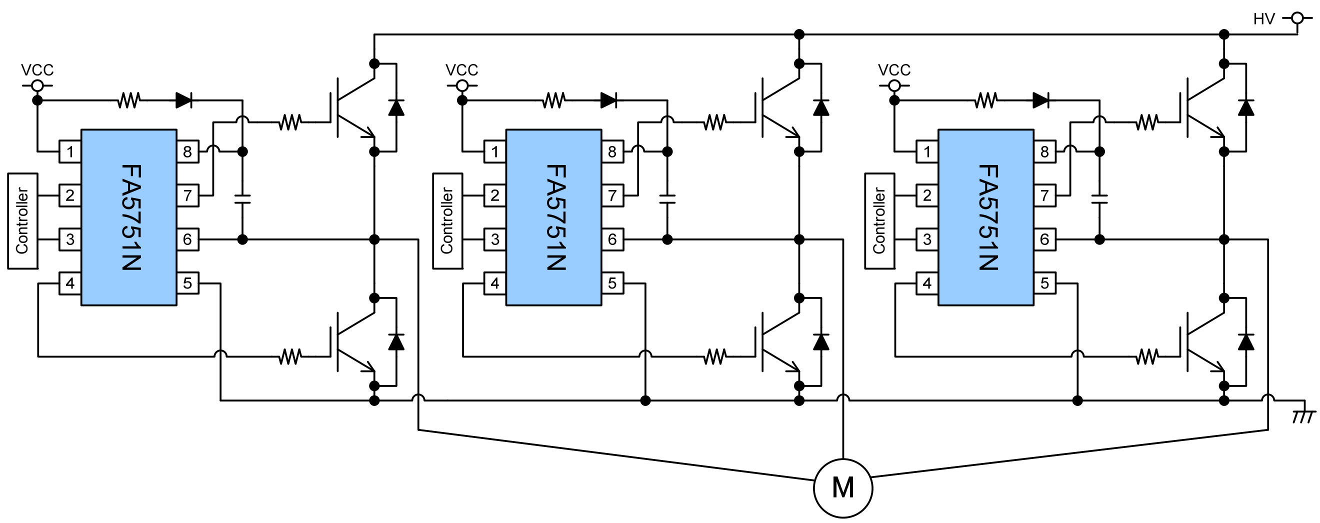
Input				Output	
HIN	**LIN**	**VCC**	**VBS**	**HO**	**LO**
-	-	L	L	L	L
-	-	L	H	L	L
-	L	H	L	L	L
-	H	H	L	L	H
L	L	H	H	L	L
H	L	H	H	H	L
L	H	H	H	L	H
H	H	H	H	H	H

When VCC or VBS increases:
“L” means the state below the ON threshold voltage.
“H” means the state above the ON threshold voltage.
When VCC or VBS decreases:
“L” means the state below the OFF threshold voltage.
“H” means the state above the OFF threshold voltage.

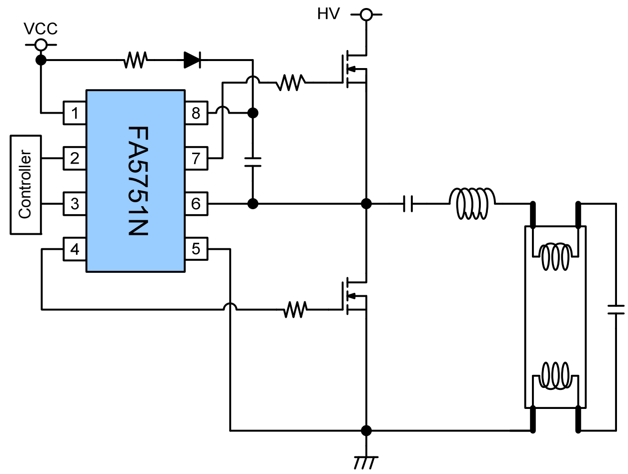
12. Typical application circuit

Typical HVIC application circuits are shown below.

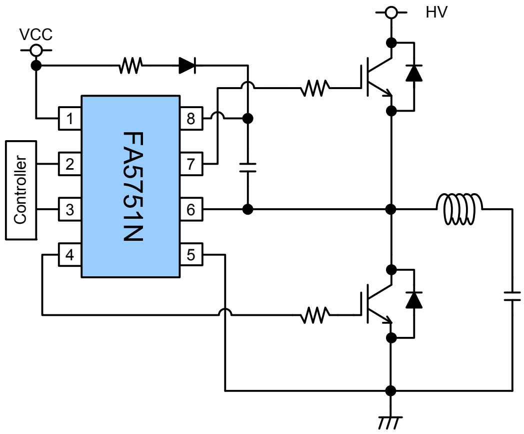
(1) Motor drive (general-purpose inverter, AC servo, air-conditioner, clothes washing machine)



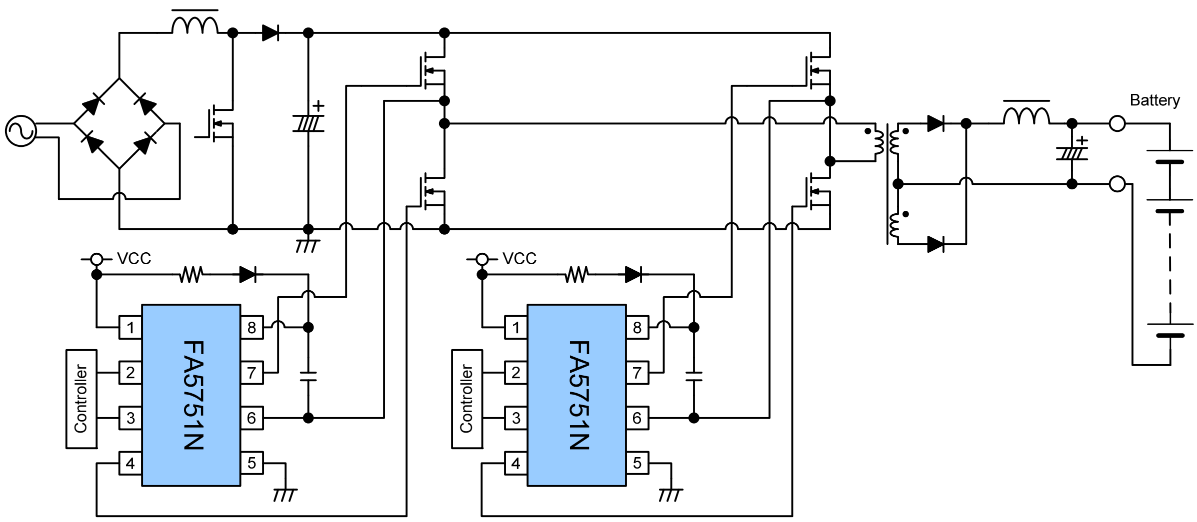
(2) Inverter fluorescent lamp



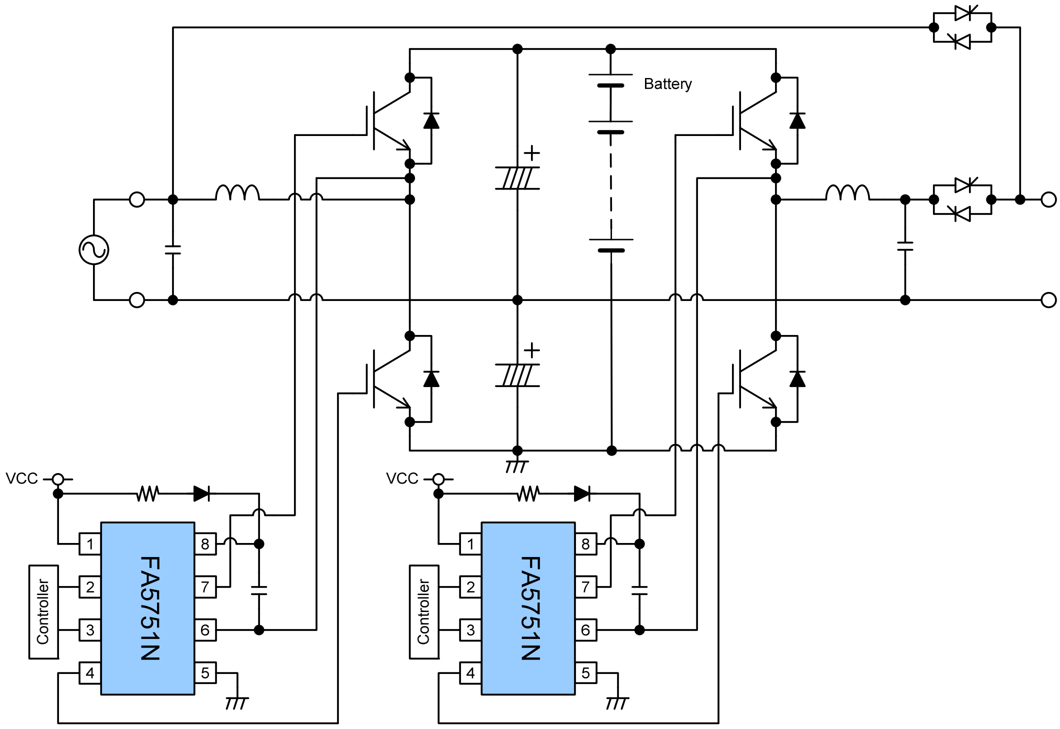
(3) IH cooking heater



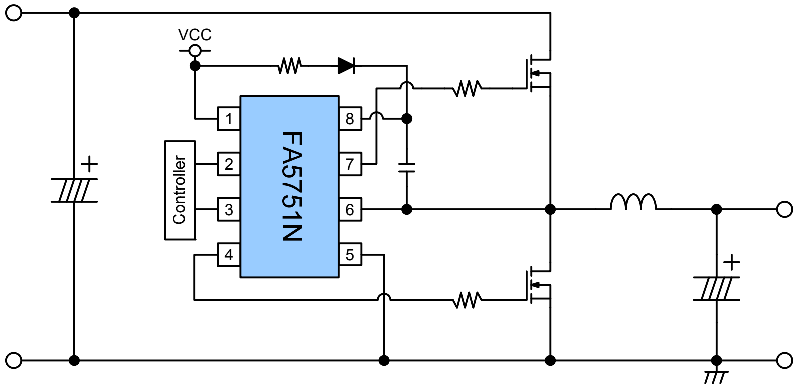
(4) AC/DC converter (battery charger)



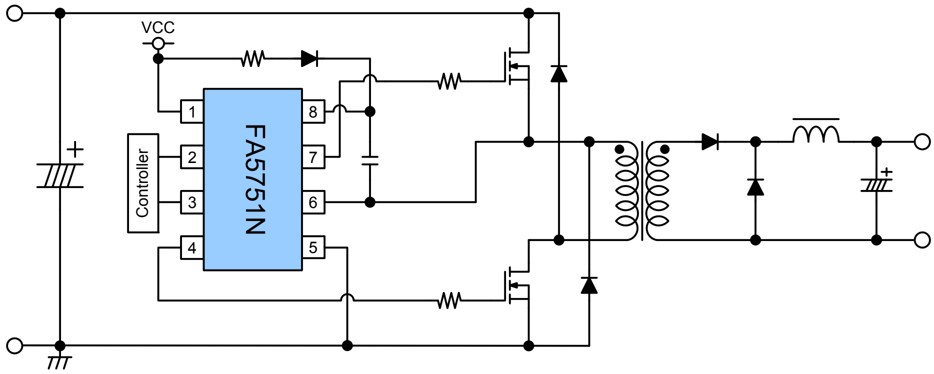
(5) UPS



(6) Buck/Boost chopper



(7) Double forward Converter

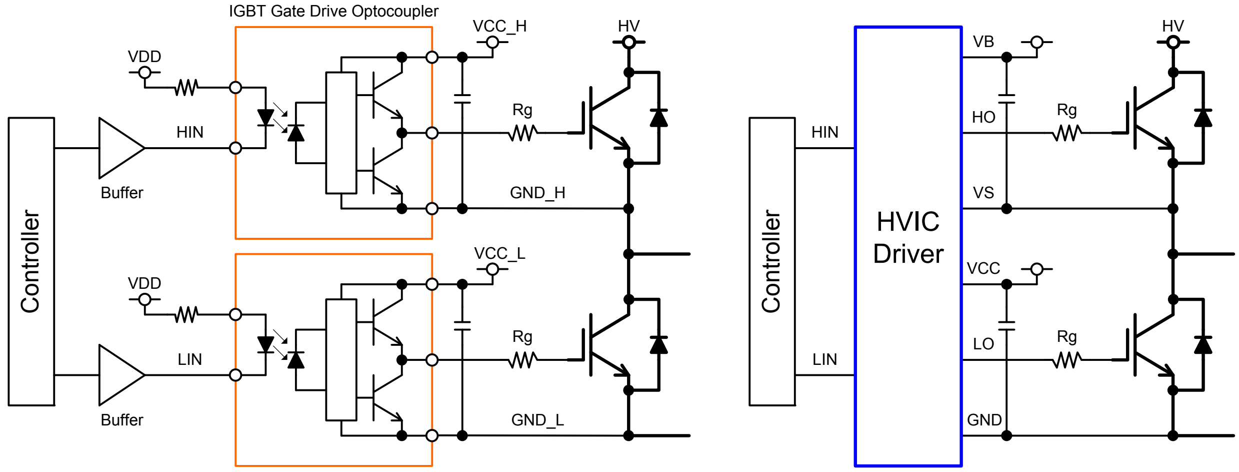


Be aware that a high-side power supply voltage made by a bootstrap circuit drops since VS voltage does not fall to GND voltage, in the case of a double forward converter circuit.

13. Compared with an Optocoupler method

In order to drive the power devices of a high-side by the control signals of a low-side, both must be insulated electrically. As the one method, an optocoupler method to insulate optically is generally used. We compare a HVIC method with a optocoupler method below.

The list below shows the difference between a HVIC method and a optocoupler method. A HVIC method has an overwhelming advantage of short signal transfer time. Therefore, HVIC suits for high-frequency switching and for fast response. And Fuji HVIC has improved the allowable negative voltage on the floating terminal VS which might cause malfunction, so it can be applied to larger power applications.



(a) Optocoupler (b) HVIC

Figure 18. Typical drive circuit with Optocoupler or HVIC

Item	Optocoupler*	HVIC (FA5751N)
Turn-on/off propagation delay	500ns (max)	170ns (max)
Propagation delay difference between turn-on and turn-off	450ns (max) | tpHL–tpLH |	90ns (max) | ton-toff |
Propagation delay difference between high and low-side	250ns (max) tpHL (max)-tpHL (min)	30ns (max) ton(High-side)-ton(Low-side)
Dead time (depends on switching characteristics of power device)	Long (2~5us)	Short (under 1us)
Switching frequency	Low speed (50kHz)	High speed (500kHz)
Allowable offset supply voltage transient	15kV/us (CMR)	50kV/us
Allowable negative voltage on the floating terminal	Good	70V (typical value)
Negative gate bias	Easy	Additional circuit is necessary
Power supply current (without gate current)	IF=10mA Icc=2mA (Vo=OPEN) x2	IBS+ICC=0.59mA

*: Typical characteristics